# RSRE
# MEMORANDUM No. 4369

# ROYAL SIGNALS & RADAR ESTABLISHMENT

## PARAMETRIC TESTING FOR THE RSRE CMOS, SILICON ON SAPPHIRE PROCESS

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R S R E MEMORANDUM No. 4369

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TITLE: PARAMETRIC TESTING FOR THE RSRE CMOS, SILICON ON SAPPHIRE PROCESS

AUTHOR: D.J. BOLLER

DATE: February 1990

## SUMMARY

This memorandum describes the parametric testing methodology implemented to evaluate the outcome of an in-house CMOS, silicon on sapphire process in its development phase. The parametric testing methodology implemented is unconventional in that it seeks to validate the assumptions made when obtaining the parameter values sought rather than assuming that they are applicable. This is achieved by associating quality factors with each of the parameters evaluated, which will only be close to their ideal values when the assumptions made are valid. In addition, the procedures used to evaluate the parameters sought and the programs subsequently employed to analyse the parametric data thus obtained do not require prior knowledge of the range of parameter values anticipated.

This methodology has been found to be of considerable value in practice, since it eliminates the need for an initial validation exercise and also checks that the assumptions which were originally made remain applicable as the process evolves. Whilst the methodology has only been implemented for a CMOS, silicon on sapphire process, it could be employed with equal effect for any other semiconductor process during its development phase.

CONTENTS

## 1.0) INTRODUCTION

This memorandum describes the structures included in the test chips used to evaluate the outcome of a CMOS, Silicon on Sapphire whole process and the methods employed to obtain and qualify the information required from them. The process has been implemented in the Silicon Process Evaluation Laboratory at RSRE and is described in RSRE memorandum 4368, "Silicon on Sapphire Device Fabrication at RSRE" by A.M. Hodge. The process has been shown to be capable of realising N and P channel devices with sub-micron channel lengths, whose characteristics are sufficiently well-behaved for use in logic circuits.

The 8501 test chip was designed in late 1984 and first used in 1985. The design rules enforced when this test chip was designed were deliberately conservative in most respects but sought to exploit the superior pattern transfer capability afforded by Direct Step on Wafer lithography and dry etching techniques. The mask set for the 8502 test chip was derived from the 8501 mask set. It includes the registration markers necessary to use E-beam lithography to define sub-micron features in the polysilicon gate layer. Additional devices have been included in the 8502 test chip which exploit this capability.

The structures included in the 8501 and the 8502 test chips are designed to facilitate the use of automated electrical measurement to acquire the information sought. The test chip is replicated over the entire wafer to reveal the spatial variations in the attributes sensed by the structures contained within it. Since each test chip contains a comprehensive range of structures which all share a common processing history, rigid process control is not necessary. This is a considerable advantage in a research and development environment, where the resources available are limited.

A sub-set of the structures included on the test chip are evaluated on a routine basis, by using a Keithley S350 Parametric Test System connected to a wafer prober. The system consists of a variety of instruments which are configured and controlled by programs run on its host computer. This system is used to perform the series of electrical measurements required to evaluate the test structures. Each of the structures included in the test chip is described by a generic equation, derived from an equivalent circuit or a theoretical model. Thus, each instance of a given structure is succinctly described by the appropriate values of the coefficients of the corresponding generic equation. The parameters utilised to compactly describe the structures are derived from these coefficients.

Clearly, the parameter values obtained on this basis are only meaningful when the characteristics exhibited by the corresponding structure can be accurately described in terms of its generic equation. Consequently, the procedures employed to obtain the parameter values sought also calculate a quality factor for each parameter evaluated. These quality factors are formulated such that they will only be close to their ideal value if the structure concerned exhibits the properties expected. The data analysis programs exploit this property to selectively exclude data obtained from any structure that does not exhibit the properties expected.

## 2.0) TEST CHIP DESIGN

A modular approach was adopted when designing the test chip. Each module is 1.6mm long by 0.3mm wide. A standardised probe pad layout is employed so that all modules can be accessed via a common probe card. This layout consists of twenty 80um square probe pads laid out in two rows of ten on a 160um pitch in both axes. The few structures that are too large to fit into a standard module are placed in dummy modules ( which have no probe pads ) and accessed via the probe pads of an adjacent module. Each chip includes additional dummy modules which contain the structures required by the Direct Step on Wafer lithography machine for alignment purposes, the optical vernier structures used to check layer to layer registration and the chip logo.

Each DSW reticle plate contains the pattern needed to define a 2x2 array of chips. This reduces the number of reticle flashes needed and improves the tolerance to defects on the reticle plates. The markers required for alignment are distributed between the two chips in the lower half of the reticle. Both dark field and light field markers have been provided. One pair of markers is defined in the epitaxial silicon layer, a second pair of markers is defined in the polysilicon gate layer, and a third pair is defined in the flow glass. Since it is not necessary to duplicate these markers in the upper half of the reticles, they have been replaced by an elongated device structure for use in cross-sectional TEM examination.

The tolerance of the probe pads to damage caused by the scrubbing action of the probe tips has been improved by forming contacts with the largest dimensions possible between the metal probe pads and isolated islands of semiconductor material, defined directly below them. The resultant probe pad is less readily scratched, because the metal is subsequently alloyed to the underlying semiconductor material.

A variety of modules has been included in the test chip. Each module has been designed to address a particular attribute of the process. There is a naturally occurring hierarchy for these modules in which an increasing reliance upon attributes that are not specifically addressed by the test structures involved becomes necessary.

The floor plan for the 8501 test chip is shown in figure 1. The contents of the modules included in this chip are briefly described in table 1.

The floor plan for the 8502 test chip is shown in figure 2. The contents of the modules included in this chip are briefly described in table 2.

The structures included in the 8501 and 8502 test chips are described in greater detail in Appendix 1. These descriptions assume some familiarity with the structures commonly used to characterise silicon processes. All of the structures are described regardless of whether they are evaluated on a routine basis or not.

Figure 1: Floor plan for the RSRE 8501 test chip

<table>
<tr><td>module 06</td><td rowspan="3">module 10</td><td>module 16</td></tr>
<tr><td>module 05</td><td>module 15</td></tr>
<tr><td>module 01</td><td>module 18</td></tr>
<tr><td>module 02</td><td>module 31</td><td>module 17</td></tr>
<tr><td>module 03</td><td>module 29</td><td>module 20</td></tr>
<tr><td>module 04</td><td>module 28</td><td>module 19</td></tr>
<tr><td>module 07</td><td>module 27</td><td>module 21</td></tr>
<tr><td>CHIP LOGO</td><td>module 32</td><td>module 22</td></tr>
<tr><td>DSW alignment</td><td>DSW alignment</td><td>DSW alignment</td></tr>
<tr><td>unused</td><td>module 14</td><td>module 23</td></tr>
<tr><td>unused</td><td>module 13</td><td>module 24</td></tr>
<tr><td>unused</td><td rowspan="3">module 33</td><td>module 25</td></tr>
<tr><td>module 09</td><td>module 26</td></tr>
<tr><td>module 08</td><td>module 11</td></tr>
<tr><td>opt. verniers</td><td rowspan="2">module 34</td><td>module 12</td></tr>
<tr><td>module 00</td><td>module 30</td></tr>
</table>

The chip size is 4.8mm by 4.8mm

Table 1: Brief description of the modules in the 8501 test chip

| Module | Brief description |
|---|---|
| 00 | Probe to module pad registration check structure |
| 01 | Metal bridge resistors: L=1020, W=2,4,6,8 and 10 |
| 02 | Poly bridge resistors: L=100, W=2,4,6,8 and 10 |
| 03 | N+ epi bridge resistors: L=100, W=5,10,15,20 plus VDP |
| 04 | P+ epi bridge resistors: L=100, W=5,10,15,20 plus VDP |
| 05 | Poly step coverage check structures plus poly VDPs |
| 06 | Metal step coverage check structures |
| 07 | Transmission line tapped resistors and contact chains |
| 08 | Inter-layer mis-alignment measurement structures, set A |
| 09 | Inter-layer mis-alignment measurement structures, set B |
| 10 | Gate oxide capacitors, rectangular and inter-digitated |
| 11 | N and P channel annular devices, edgeless and slotted |
| 12 | Long N and P channel devices: L=40, W=10,130 and 250 |
| 13 | N channel devices with varied orientation: L=50, W=50 |
| 14 | P channel devices with varied orientation: L=50, W=50 |
| 15 | N channel devices: L=1,2,3,4,5 and 10, W=10 |
| 16 | P channel devices: L=1,2,3,4,5 and 10, W=10 |
| 17 | N channel devices: L=1,2,3,4,5 and 10, W=2 |
| 18 | P channel devices: L=1,2,3,4,5 and 10, W=2 |
| 19 | N channel devices: L=1,2,3,4,5 and 10, W=40 |
| 20 | P channel devices: L=1,2,3,4,5 and 10, W=40 |
| 21 | N channel devices: L=2.5,2.7,2.9,3.1,3.3 and 3.5, W=10 |
| 22 | P channel devices: L=2.5,2.7,2.9,3.1,3.3 and 3.5, W=10 |
| 23 | N channel devices, Kelvin S/D: L=3, W=10,20,30 and 40 |
| 24 | P channel devices, Kelvin S/D: L=3, W=10,20,30 and 40 |
| 25 | N channel devices, Kelvin S/D: L=3, W=2,4,6 and 8 |
| 26 | P channel devices, Kelvin S/D: L=3, W=2,4,6 and 8 |
| 27 | Eighteen N channel devices in close proximity: L=3, W=10 |
| 28 | Eighteen P channel devices in close proximity: L=3, W=10 |
| 29 | N and P channel gate controlled VDPs, varied orientation |
| 30 | N and P channel substrate contacted devices |
| 31 | N and P channel Hall bar structures |
| 32 | Miscellanous circuit elements |
| 33 | 16 bit synchronous shift register circuit |
| 34 | Various 3-input gates |

The dimensions ( where stated ) are nominal, in micron units.

| Abbreviation | Explanation |
|---|---|
| poly | polysilicon, heavily doped N type |
| epi | Epitaxial silicon, grown on the sapphire substrate |
| S/D | Source and drain regions |
| N+ epi | epi that has received the N channel S/D implant |
| P+ epi | epi that has received the P channel S/D implant |
| VDP | Van der Pauw resistor structure |
| Kelvin S/D | Kelvin connections made to the source/drain regions |

Figure 2: Floor plan for the RSRE 8502 test chip

<table>
<tr><td>module 06</td><td rowspan="3">module 10</td><td>module 16</td></tr>
<tr><td>module 05</td><td>module 15</td></tr>
<tr><td>module 01</td><td>module 18</td></tr>
<tr><td>module 02</td><td>module 31</td><td>module 17</td></tr>
<tr><td>module 03</td><td>module 29</td><td>module 20</td></tr>
<tr><td>module 04</td><td>module 28</td><td>module 19</td></tr>
<tr><td>module 07</td><td>module 27</td><td>module 21</td></tr>
<tr><td>CHIP LOGO</td><td>module 32</td><td>module 22</td></tr>
<tr><td>DSW alignment</td><td>DSW alignment</td><td>DSW alignment</td></tr>
<tr><td>module 35</td><td>module 14</td><td>module 23</td></tr>
<tr><td>module 36</td><td>module 13</td><td>module 24</td></tr>
<tr><td>module 37</td><td rowspan="3">module 33</td><td>module 25</td></tr>
<tr><td>module 09</td><td>module 26</td></tr>
<tr><td>module 08</td><td>module 11</td></tr>
<tr><td>opt. verniers</td><td rowspan="2">module 34</td><td>module 12</td></tr>
<tr><td>module 00</td><td>module 30</td></tr>
</table>

The chip size is 4.8mm by 4.8mm

Table 2: Brief description of the modules in the RSRE 8502 test chip

| Module | Brief description |
|---|---|
| 00 | Probe to module pad registration check structure |
| 01 | Metal bridge resistors: L=1020, W=2,4,6,8 and 10 |
| 02 | Poly bridge resistors: L=100, W=2,4,6,8 and 10 |
| 03 | N+ epi bridge resistors: L=100, W=5,10,15,20 plus VDP |
| 04 | P+ epi bridge resistors: L=100, W=5,10,15,20 plus VDP |
| 05 | Poly step coverage check structures plus poly VDPs |
| 06 | Metal step coverage check structures |
| 07 | Transmission line tapped resistors and contact chains |
| 08 | Inter-layer mis-alignment measurement structures, set A |
| 09 | Inter-layer mis-alignment measurement structures, set B |
| 10 | Gate oxide capacitors, rectangular and inter-digitated |
| 11 | N and P channel annular devices, edgeless and slotted |
| 12 | N and P channel devices: L=40, W=10,130 and 250 |
| 13 | N channel devices with varied orientation: L=50, W=50 |
| 14 | P channel devices with varied orientation: L=50, W=50 |
| 15 | N channel devices: L=1,2,3,4,5 and 10, W=10 |
| 16 | P channel devices: L=1,2,3,4,5 and 10, W=10 |
| 17 | N channel devices: L=1,2,3,4,5 and 10, W=2 |
| 18 | P channel devices: L=1,2,3,4,5 and 10, W=2 |
| 19 | N channel devices: L=1,2,3,4,5 and 10, W=40 |
| 20 | P channel devices: L=1,2,3,4,5 and 10, W=40 |
| 21 | N channel devices: L=2.5,2.7,2.9,3.1,3.3 and 3.5, W=10 |
| 22 | P channel devices: L=2.5,2.7,2.9,3.1,3.3 and 3.5, W=10 |
| 23 | N channel devices, Kelvin S/D: L=3, W=10,20,30 and 40 |
| 24 | P channel devices, Kelvin S/D: L=3, W=10,20,30 and 40 |
| 25 | N channel devices, Kelvin S/D: L=3, W=2,4,6 and 8 |
| 26 | P channel devices, Kelvin S/D: L=3, W=2,4,6 and 8 |
| 27 | Eighteen N channel devices in close proximity: L=3, W=10 |
| 28 | Eighteen P channel devices in close proximity: L=3, W=10 |
| 29 | N and P channel gate controlled VDPs, varied orientation |
| 30 | N and P channel substrate contacted devices |
| 31 | N and P channel Hall bar structures |
| 32 | Miscellanous circuit elements |
| 33 | 16 bit synchronous shift register circuit |
| 34 | Various 3-input gates |
| 35 | N and P channel devices: L=1.0,0.75 and 0.5, W=10 |
| 36 | N and P channel devices: L=1.0,0.75 and 0.5, W=2 |
| 37 | N and P channel devices, L=0.5,0.375 and 0.25, W=2 |

The dimensions ( where stated ) are nominal, in micron units

| Abbreviation | Explanation |
|---|---|
| poly | polysilicon, heavily doped N type |
| epi | Epitaxial silicon, grown on the sapphire substrate |
| S/D | source and drain regions |
| N+ epi | epi that has received the N channel S/D implant |
| P+ epi | epi that has received the P channel S/D implant |
| VDP | Van der Pauw resistor structure |
| Kelvin S/D | Kelvin connections made to the source/drain regions |

## 3.0) PARAMETRIC DATA ACQUISITION

The on-wafer test system employed consists of a Keithley S350 Parametric Test System and an Electroglas model 2001X wafer prober, both controlled by programs run on a PDP11/84 minicomputer. These programs are described as parametric data acquisition programs. Each program controls the wafer prober in order to access each of the modules required in turn. They use the switching matrix within the S350 Parametric Test System to configure its instruments as necessary and connect them to the appropriate probes, so that the structure in question can be evaluated. The S350 instruments are then used to perform the series of measurements required to evaluate both the parameter values sought and the quality factors associated with them.

The parameter values required are derived by evaluating the coefficients of the generic equation which is utilised to describe the characteristic exhibited by the structure in question. This generic equation is derived from an equivalent circuit or a theoretical model. It therefore involves a number of assumptions, which are not necessarily valid. The concept of a quality factor has been introduced, in order to provide an independent measure of the validity of these assumptions. The measurement procedures utilised evaluate the parameter values sought on the assumption that the appropriate generic equation is applicable, but they also obtain a value for the quality factor associated with each of the parameter values thus obtained. The values assigned to these quality factors are subsequently utilised to identify structures whose characteristic did not exhibit the properties expected. The parameter values obtained from these structures are ignored on the basis that they are unlikely to be meaningful.

The use of quality factors is not merely a complicated method of sorting the chaff from the wheat. The quality factors obtained for all instances of a given structure should be close to their ideal value if the generic equation is applicable regardless of the corresponding parameter values. Thus, they can also be used to validate the assumptions made in order to obtain the parameter values required.

The parametric data acquisition programs for the 8501 or 8502 test chips are identified by the name given to the wafer pass performed. Each wafer pass obtains specific information from a sub-set of the modules included in the test chip. Wafer pass A evaluates the structures contained within modules 01 to 07 inclusive. The key attributes of the individual layers and the front resistances which characterise the three kinds of metal to semiconductor contacts required are evaluated during this wafer pass.

Wafer pass B was intended to investigate the accuracy of the system used by the Direct Step on Wafer lithography machine to align each reticle to the pattern previously transferred to the wafer. The structures included in modules 08 and 09 could be used for this purpose. However, it has not been coded because in-process monitoring ( using the optical verniers on the test chip ) indicates that the alignment achieved by this machine is entirely satisfactory.

Wafer pass C was intended to evaluate Cox from the rectangular capacitor structures included in module 10 and then evaluate the dependence of the effective carrier mobility values upon the direction of current flow, by using the devices with varied orientation included in modules 13 and 14. It has not been coded yet, because this effect was not deemed to be very significant.

Wafer pass D is considered to be obsolete and has not been documented in in this memorandum. It has been replaced by wafer pass E.

The families of devices of varied length, which are contained in modules 15, 16, 17, 18, 19 and 20, are investigated during wafer pass E. The Ids versus Vgs characteristics exhibited by these devices when the magnitude of Vds is small are obtained. The devices operate in their triode region for the majority of the gate bias values applied. Hence, the appropriate portion of this characteristic is used to evaluate the parameters VROOT, BETAO and THETA. The parameter VROOT is equal to the root of the triode equation and tracks any threshold voltage variation. The parameter BETAO is the gain factor which is proportional to the width of the channel and inversely proportional to its length. The parameter THETA describes the curvature of the Ids versus Vgs characteristic due to the net effect of transverse electric field scattering and the resistances associated with the source and drain regions. The length dependences of these parameters are then described by three additional pairs of parameters, which reveal the channel length reduction due to the net effect of sideways diffusion of the self-aligned source and drain implants and reduction in the width of the gate electrode due to linewidth loss during pattern transfer, the sensitivity of the threshold voltage to changes in the effective channel length and the significance of the parasitic resistances associated with the source and drain regions.

Wafer pass F performs a similar function to wafer pass E, but utilises a more elaborate method to evaluate parameters VROOT, BETAO and THETA. The fit to the measured characteristic is improved considerably, as a result of the method employed to optimise the value assigned to VROOT.

## 3.1) PARAMETRIC DATA ACQUISITION PROGRAM STRUCTURE

The information required from each wafer is obtained by running a number of parametric data acquisition programs. Each program acquires data from the test structures defined within a unique set of modules and creates a file in which the data is saved. These files are managed by the database management software.

The parametric data acquisition programs all involve two distinct phases of operation. During the set-up phase, they establish the "key strings" needed to keep track of the data files created, generate the "map" which specifies whether each chip defined on the wafer is to be visited during the wafer pass or not, set-up the wafer prober and instruct the operator to align the wafer as required. During the wafer pass phase, they visit each chip specified in the "map", access the appropriate set of modules within each chip in turn and acquire the parametric data sought from the test structures thus accessed.

The wafer prober is capable of moving its X,Y stage to any location on a rectangular grid. The pitch between adjacent locations in X is described as the X axis index displacement value whilst the pitch between adjacent locations in Y is described as the Y axis index displacement value. Once the coordinates for the current location have been specified, the wafer prober can be instructed to move to the location defined by a new set of coordinates as required.

The programs used to acquire parametric data all require that the prober can move between the various chips on each wafer and between the modules within the chip currently accessed as necessary. Consequently, two grids are required; one in which each location corresponds to the registration check module of each chip defined on the wafer, and another in which the locations correspond to the various modules defined on a given chip. The ability to program the index displacement values to be used by the wafer prober when moving between locations and to reset the X,Y coordinates as required is crucial to the implementation of these tasks. By instructing the operator to align the probes to the registration check module of any convenient chip and then asking the operator to specify its coordinates, the current location of the X,Y stage, within each of the grids defined, is known. The index displacement values needed to move between the chips on the wafer and those required to move between modules within each chip are also known.

The "key strings" needed to keep track of the data files created are all fixed length character strings. The significance of each "key string" is as follows:

| | |
|---|---|
| 1) Wafer I/D: | unique for each wafer processed |
| 2) Job Number: | unique for each batch of wafers |
| 3) Schedule: | names the process schedule document |
| 4) Wafer Map: | defines the set of chips accessed |
| 5) Wafer Pass: | defines the set of modules accessed |

The Wafer I/D, Job Number and Schedule are entered by the operator using information supplied by the processing laboratory. The Wafer Map defines the set of chips to be accessed during the wafer pass, by specifying the

name of an existing file which contains the information used to generate a "map". This "map" contains an entry for each chip defined on the wafer which specifies if it is to be visited during the wafer pass or not. By including the Wafer Map in the set of "key strings" used to identify the files created by the parametric data acquisition programs, it is easy to associate the files resulting from different parametric data acquisition programs which accessed the same set of chips during their wafer passes. Each parametric data acquisition program assigns a unique identification string to the Wafer Pass "key string", since it is necessary to identify the source of each "log" file created ( the database management software uses this "key string" to generate the name of the file which contains a descriptive text string for each of the parameter values recorded ).

The operator is then instructed to set-up the wafer prober and align the probes to the wafer as necessary, enter the coordinates of the chip used for this alignment and then switch off the microscope illuminator on the wafer prober, in readiness for the wafer pass. On receiving confirmation that this has been done, the programs open a "log" file which is used to save the parametric data obtained and record the values assigned to each of the "key strings" at the beginning of the "log" file.

The wafer pass commences with the X,Y stage of the wafer prober at known chip coordinates and at known module coordinates. The X and Y axis index displacement values are set to suit movements between chips on the wafer and the prober's coordinates are set so that they correspond to those of the chip used by the operator when aligning the probes to the wafer. The programs identify those chips that are to be visited during the wafer pass by testing each element of the "map" array in turn. As each chip is identified, the programs cause the wafer prober to move its X,Y stage to the appropriate chip coordinates and raise its wafer chuck to access the registration check module ( i.e. module 00 ).

The programs check the alignment of the probes to the wafer for the chip currently being visited by calling the registration check procedure. The registration check procedure performs a series of continuity tests which is designed to identify which probes, if any, have failed to "hit" their probe access pads and sets the pass/fail status flag accordingly. If any of the probes has failed to "hit" its probe access pad, the registration check procedure issues an appropriate report to the operator's terminal. The coordinates of the chip in question, the status flag returned by the registration check procedure and the number of modules to be accessed in turn ( before the next chip is visited ) are recorded in the "log" file.

In order to access the various modules required within the current chip, the programs set the X and Y axis index displacement values so that they are suitable for movement between modules and set the prober coordinates such that they correspond to the module coordinates for the registration check module. Then, they access each of the modules required in turn, by causing the wafer prober to move its X,Y stage to the appropriate module coordinates, and call a procedure which is specific to that module. Each procedure is responsible for acquiring the parametric data sought from a specific module and recording the data obtained in the "log" file. These procedures are required to record the number of parameters obtained then to record each parameter value, its corresponding quality factor and its corresponding encoded status word in successive records.

When all of the parametric data sought has been acquired from this chip, the programs then cause the wafer prober to return its X,Y stage to the registration check module leaving the wafer chuck lowered, set the X and

Y axis index displacement values so that they are suitable for movement between chips, and set the wafer prober coordinates to correspond to the current chip coordinates. They are then ready to locate the next chip to be visited and repeat the sequence of operations described.

Once all of the chips defined in the "map" have been visited and all the parametric data sought has been acquired, the programs close their "log" file and exit. The data contained within this file is subsequently added to the database by running the database load utility task.

## 3.2) WAFER PASS A

### 3.2.1) Introduction

This wafer pass evaluates all of the structures contained in modules 01, 02, 03, 04, 05, 06 and 07. Module 01 evaluates the sheet resistivity for the metal layer and the linewidth loss for its pattern transfer process. The sheet resistivity of the metal layer serves as a thickness analogue, since the bulk resistivity of the metal is expected to be uniform due to its purity. Module 02 evaluates the sheet resistivity and the linewidth loss for the doped poly layer. Since the poly is degenerately doped, its sheet resistivity can also be treated as a thickness analogue. The front resistance for metal to poly contacts will also be affected by variation in the poly sheet resistivity. Module 03 evaluates the sheet resistivity and linewidth loss for epi which has received the N channel source/drain implant ( N+ epi ), whilst module 04 evaluates the sheet resistivity and the linewidth loss for epi which has received the P channel source/drain implant ( P+ epi ). Variation in the sheet resistivity of either the N+ or P+ epi is relatively difficult to interpret since it can be caused by a number of factors. The linewidth loss values obtained from modules 03 and 04 are expected to be similar, since the source/drain implants occur after the epi pattern transfer has been performed. Module 05 evaluates the changes in the sheet resistivity for the doped poly layer due to the dopant received during the self-aligned source/drain implants. Module 05 also includes structures designed to detect poly step coverage problems. Module 06 includes structures designed to detect any metal step coverage problems. Module 07 evaluates the front resistance for metal contacts to N+ epi, P+ epi and poly respectively and includes chains of 100 contacts for each type of contact.

With the exception of the contact test structures in module 07, the test structures evaluated by wafer pass A all use 76um square contacts formed directly below the corresponding probe access pad. This ensures that the contacts will be maximally tolerant to a high interfacial layer specific resistivity. In addition, Kelvin connections have been made so that they do not even require the existence of an ohmic contact. The structures in module 07 are designed to evaluate 6um square ( minimum geometry ) metal to semiconductor contacts. Evidently, they do require a low interfacial layer specific resistivity if the contacts evaluated are to exhibit the low front resistance values sought.

There are five distinct types of test structure to be evaluated in wafer pass A. These are:

1) 4-terminal bridge resistor structures

2) Van der Pauw resistor structures

3) Step coverage check structures

4) Transmission line tapped resistor structures

5) Contact chain structures

Specific procedures are provided for each of the five types of structure evaluated. Since each of these procedures makes use of 2-terminal and/or 4-terminal resistance measurements, they utilise generalised procedures which perform the necessary operations.

### 3.2.2) Generalised 2-terminal resistance measurement procedure

Procedure R2V is used to perform the 2-terminal resistance measurements. It assumes that the load is resistive and seeks to quantify the slope of the V/I characteristic exhibited whilst honouring a maximum power limit. The power delivered to the load is supplied by a programmable V/I source which can be programmed to operate either in a voltage source mode or in a current source mode. When the V/I source is programmed to operate as a voltage source, the maximum output current can be programmed and when it is programmed to operate as a current source, the maximum output voltage can be programmed. The V/I source automatically switches between its two operating modes according to the load encountered. Evidently, its output impedance changes dramatically when it switches between modes. R2V uses the V/I source in its voltage source mode, but measures both the current through the load and the voltage actually applied. This ensures that the measurement is accurate even if the V/I source is current limited. Since the current meter LO must be connected to ground if the current measured is to be accurate, the current meter is connected to complete the return path. Thus, the load is connected between the V/I source HI terminal and the current meter HI terminal ( which is at ground potential ). By using the voltage source mode, the voltage applied can be set to the smallest value consistent with an accurate voltage measurement, whilst maximising the current permissible for a given output power limit. This will ensure that the V/I source operates in its voltage source mode, unless the load has an extremely low resistance. Thus, accuracy is preserved over a wide range of V/I ratios. R2V defines the 2-terminal resistance as the slope of a straight line drawn between two points on the V/I characteristic of the load. The first point is obtained by programming a positive voltage of the specified magnitude, subject to a current limit determined by the maximum power permissible, and the second point is obtained by reversing the polarity of the programmed voltage. Both the current and the voltage are measured for each programmed output voltage. R2V also calculates the voltage necessary to result in no current through the load. This offset, which should be extremely small if the V/I characteristic of the load is bilateral, is used as the quality factor for this measurement. Also, R2V returns an encoded status word which flags the occurence of events which may have compromised the measurement.

### 3.2.3) Generalised 4-terminal resistance measurement procedure

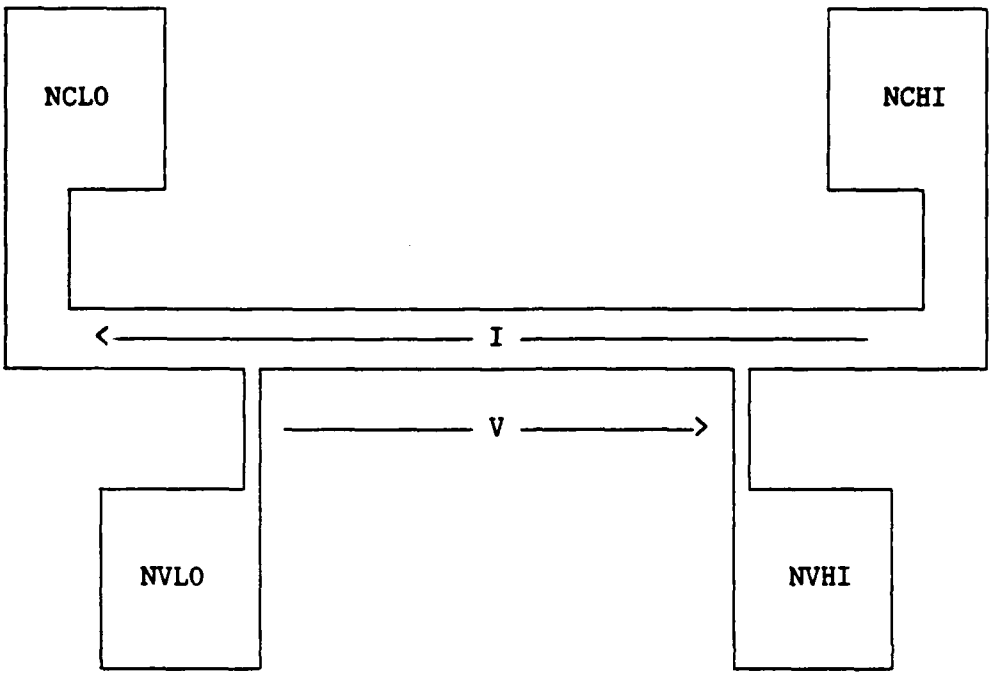
Procedure R4V is utilised to perform 4-terminal resistance measurements. For the purposes of this procedure, the four terminal structure involved is considered to be a 2-port network where the voltage developed between its output terminals is expected to be a linear function of the current flowing between its input terminals. The 4-terminal resistance value is determined from the slope of this transfer characteristic. Although the test structures involved have been designed so that they should exhibit a linear transfer characteristic, R4V seeks to evaluate the slope of the transfer characteristic ( assuming linearity ) and quantifies the degree of non-linearity exhibited. However, many of the test structures include contacts in the current path through their input port and in the current path through their output port. Thus, the V/I characteristics for these two ports are not necessarily linear. The effect of any non-linearity in the V/I characteristic of the input port can be minimised by using a V/I source in its current source mode to directly control the current forced through it. The effect of any non-linearity in the V/I characteristic of the output port is negligible, since the differential voltmeter employed to measure the resultant response has extremely low input bias currents. During the measurement procedure, R4V limits the maximum power output by

the V/I source by controlling its maximum output voltage. Consequently, it is necessary to use the current meter to measure the current actually flowing through the input port in case the V/I source becomes compliance limited. Since a low resistance path has to be provided between current meter LO terminal and ground to guarantee accurate current measurements, it is connected in the current return path. The 4-terminal resistance is calculated from the slope of a straight line drawn between two measured points on the transfer characteristic. The points are chosen to maximise the accuracy of the measurements, whilst minimising the power dissipated in the test structure. These requirements are best satisfied by forcing the least current necessary to develop a voltage which can be accurately measured by the voltmeter. The optimum current value is determined by an iterative procedure in which the data obtained from the previous attempt is used to predict the current necessary to achieve the target value for the output voltage. The first current value attempted is set so that the voltage applied to the input port should be equal to the target value of the output voltage. R4V requires that the 2-terminal resistance for the input port has been measured by a previous call to R2V ( this is done as part of the integrity checks performed before calling R4V ) to calculate this initial current value. The V/I source is programmed to source this current and both the current actually flowing through the input port and the resultant output voltage are measured and used to predict an optimum current value for the next attempt. An ohmic transfer characteristic is assumed for this prediction, provided that the output voltage is greater than 10% of the target value. Otherwise, the programmed current value is increased by a factor of ten. This avoids a gross overshoot due to error in the measurement of a relatively small voltage. This iterative process is considered to be successful if the output voltage is within 1% of the target value specified. This normally takes relatively few iterations to achieve. Since it is conceivable that R4V could become stuck in a limit cycle, the number of iterations is limited to twenty. Although it could be assumed that the transfer characteristic passes through the origin, a second point on the V/I characteristic is obtained instead. This is done by reversing the polarity of the programmed current value then repeating the voltage and current measurements. The slope of a straight line drawn between these two points is calculated. The 4-terminal resistance value returned, R4TERM, is equal to this value. To evaluate the non-linearity of the transfer characteristic, R4V measures two additional points using positive and negative programmed current values, whose magnitude is half that used to determine R4TERM. These points are used to determine RCHECK by evaluating the slope of a straight line drawn between them. These two 4-terminal resistance values will be in close agreement, if the transfer characteristic exhibits the degree of linearity expected. R4V calculates a non-linearity factor which is defined as ( R4TERM - RCHECK ) / R4TERM. The quality factor for the 4-terminal resistance measurement returned by R4V is set equal to this non-linearity factor. In addition, R4V returns an encoded status word. The 16 bits of this word are used to flag events which may have compromised the accuracy of the measurement. If R4V found it necessary to abort, bit 15 of the encoded status word is set. This is only necessary if R4V appears to be stuck in a limit cycle or to avoid a divide by zero error. If R4V does have to abort, it will return default values for the 4-terminal resistance and its quality factor.

3.2.4) Bridge resistor measurement procedure

Procedure KELVIN is called to evaluate the resistance that characterises the 4-terminal bridge resistor structures. Bridge resistors are defined either in metal, unimplanted poly, N+ epi or P+ epi. Unimplanted poly is poly that has been heavily doped N type, but has not received either the

N or the P channel source/drain implant dose. The N+ epi material is epi that has received the N channel source/drain implant dose, whilst the P+ epi material is epi that has received the P channel source/drain implant instead. A schematic diagram for the bridge resistor structure is shown below:




where "NCLO", "NVLO", "NVHI" and "NCHI" represent the probe access pads for the bridge resistor structure evaluated by procedure KELVIN.

The resistance value sought defines the slope of the V/I characteristic, which is expected to be linear. When metal to semiconductor contacts are required, they are formed directly below the probe access pads. Thus, it is anticipated that the characteristic will be linear, provided that the conductive sheet, in which the body of the resistor is defined, exhibits ohmic behaviour. Procedure R4V is utilised to evaluate this resistance. It is necessary to check the 2-terminal resistance measured between NVHI and NVLO before calling R4V since an open-circuit would cause it to come to grief. Also, the 2-terminal resistance measured between NCHI and NCLO is required so that it can be passed to R4V. KELVIN makes two successive calls to R2V to obtain the values required. If either of these values is in excess of one megohm, the 4-terminal resistor structure is considered to be defective. In this event, KELVIN returns a default value for both the 4-terminal resistance value sought and the quality factor associated with it. KELVIN also returns an encoded status word. The sixteen bits of this word are utilised to flag any events which may have compromised the accuracy of the results obtained. Bit 15 of this word is set when KELVIN was not able to evaluate the 4-terminal resistance required.

3.2.5) Deriving sheet resistivity and linewidth loss

By defining a family of bridge resistor structures in a given conductive layer, where the structures differ only in that their nominal widths are varied, the sheet resistivity and the linewidth loss can be deduced from

conductance versus nominal width data. Families of bridge resistors are defined in metal ( module 01 ), in unimplanted poly ( module 02 ), in N+ epi ( module 03 ) and in P+ epi ( module 04 ). Each bridge resistor uses voltage sensing taps to sense the voltage developed along a known length of a conductive strip whose nominal width is known. If all of the bridge resistors in a given family suffer the same loss in linewidth during the pattern transfer process, the conductance values exhibited are expected to be proportional to the nominal width minus the ( constant ) linewidth loss term and inversely proportional to the sheet resistivity. Thus, the sheet resistivity and the linewidth loss term for the layer involved can be deduced from the coefficients of a least squares straight line fit to the measured conductance values versus the corresponding nominal width.

The conductance of a given bridge resistor is described by the equation:

$$G = ( WNOM - DELTAW ) / ( LNOM * RSHEET )$$

where: WNOM is the nominal width of the bridge resistor

DELTAW is the ( constant ) linewidth loss term

LNOM is the distance between the voltage sensing taps

and: RSHEET is the sheet resistivity for the layer

Whilst this equation assumes that width of the voltage sensing taps tend to zero, the effect of their finite width is minimised by the relatively large value of LNOM. Thus, any errors due to perturbation of the current flux in the vicinity of the voltage sensing taps are discounted.

The procedure utilised to perform the least squares straight line fit is such that the values of the dependent variables can be weighted in order to account for their relative uncertainty if required. It calculates the coefficients of the least squares straight line which result in the best fit, by minimising the sum of the weighted deviations, and evaluates the resultant linear correlation coefficient.

Whilst the conductance values exhibit a very strong correlation with the corresponding nominal width values, the choice of weighting coefficients for the dependent variable does affect the outcome somewhat. In general, the dispersion is greater than that expected from instrumentation errors alone. The dispersion exhibited by the data could be due to variation in the sheet resistivity or variation in the linewidth loss for each bridge resistor in the family. If the dispersion is solely due to variation in the linewidth loss term, then it would be appropriate to assume that the uncertainty in the values of the dependent variable are equal. However, if the dispersion is solely due to variation in the sheet resistivity of the layer in which the bridge resistors are delineated, then it would be appropriate to assume that the uncertainty in the value of the dependent variable is proportional to the value itself. Although it is likely that the dispersion observed is due to a combination of these effects, it has been found that the linear correlation coefficient is slightly nearer to the ideal value ( unity ) when the uncertainty in the dependent variable is assumed to be proportional to the value obtained.

The sheet resistivity and the linewidth loss term for a given conductive layer is based upon the assumption that the conductivity of the layer is unaffected by the existence of "sidewalls" along the edges of the bridge resistor structures. In practice, the conductivity of these "sidewalls"

may differ from that exhibited by the "body" ( i.e. the remainder of the structure ). It is anticipated that the sheet resistivity value obtained from the family of bridge resistor structures will correspond to that of the "body". However, a difference in the conductivity of the "sidewalls" and the "body" would result in an error in the linewidth loss term. This error would be particularly severe if current flows preferentially along the "sidewalls". In this event, the conductivity of the bridge resistors would be substantially independent of their nominal widths ( which would result in a physically unrealistic linewidth loss term ). Although there is no independent test for the existence of a preferential current path along the "sidewalls", Van der Pauw resistor structures are included for each type of semiconductor layer which provide a means of detecting such paths. This is discussed later. Evidently, no such problems are expected in respect of the family of bridge resistor structures which are defined in the metal layer. Also, it is unlikely that there will be any problems due to differences in the conductivity of the "sidewalls" and the "body" for the bridge resistors defined in the semiconductor layers, since they are so heavily doped that their conductivity will not be affected by the surface potential. Nevertheless, the chances of encountering problems of this nature cannot be eliminated altogether.

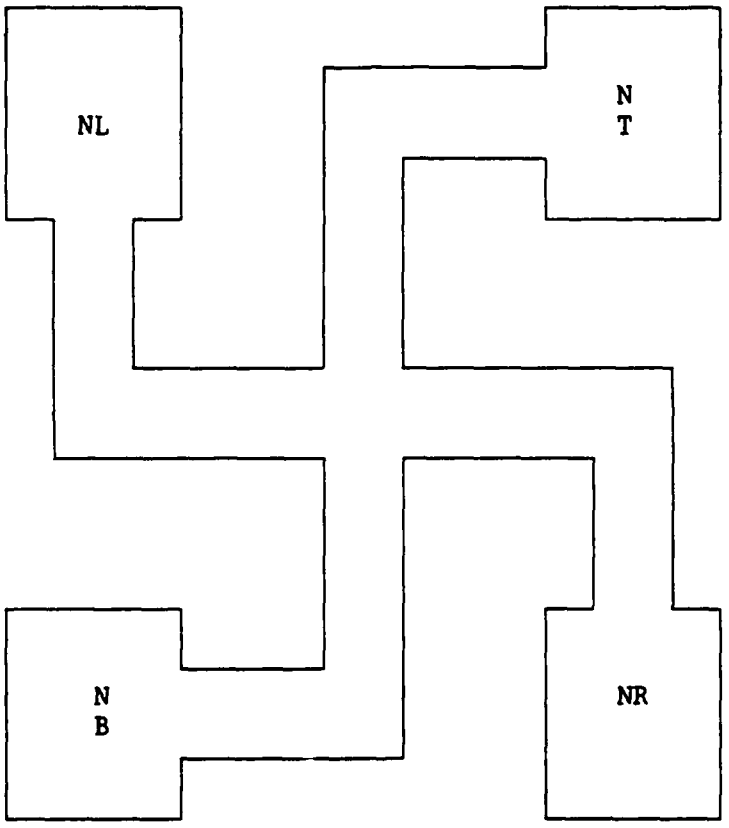
The linewidth loss term is only meaningful if the edges that are defined during pattern transfer are very nearly vertical. If they are not, then the variation in the conductivity of the layer with depth is expected to affect the linewidth loss term obtained. In particular, one would expect that the linewidth loss term obtained from the family of bridge resistor structures defined in N+ epi to agree with that obtained from the family defined in P+ epi, since these structures receive their dopant after the pattern has been delineated in the epi as required.

The sheet resistivity and the linewidth loss term for a given conductive layer are computed by the procedures which are called to evaluate all of the structures within the module in which the family of bridge resistors are included. The procedures obtain values for the 4-terminal resistance which characterise each bridge resistor in turn by calling KELVIN, which also returns a quality factor and an encoded status word for each bridge resistor. They utilise the encoded status words to determine whether the corresponding 4-terminal resistance value returned by KELVIN is valid or not ( specified by bit 15 ). An entry is made in arrays that contain the conductance values ( the reciprocal of the 4-terminal resistance value ) and the corresponding nominal widths for each valid result. If there are at least three valid results, they perform a least squares straight line fit as required and then compute the sheet resistivity and the linewidth loss term from the coefficients of the straight line fitted. The linear correlation coefficient, computed by the least squares straight line fit procedure, serves as the quality factor for both of these parameters. If this is not possible, default values are assigned to both parameters and to their corresponding quality factors. The corresponding encoded status words for each of these parameters are set equal to the number of valid results obtained for the family of bridge resistor structures and bit 15 is set if the number of valid results obtained is less than three ( this indicates that default parameter values have been assigned instead ).

### 3.2.6) Van der Pauw resistor measurement procedure

Procedure VDP is used to evaluate the sheet resistivity for a conductive sheet in which a Van der Pauw resistor structure has been defined. These structures are delineated in semiconductor material whose doping density is sufficiently high to ensure that its sheet resistivity is independent

of its surface potential. Van der Pauw resistor structures are provided to evaluate the sheet resistivity for N+ epi, P+ epi, N+ implanted poly, P+ implanted poly and unimplanted poly respectively. The N+ epi material is epi which has received the N channel source/drain implant dose whilst the P+ epi material has received the P channel source/drain implant dose instead. All poly is heavily doped N type prior to pattern transfer. The N+ implanted poly material and the P+ implanted poly material receive an additional dopant dose, due to the N and P channel source/drain implants respectively. The unimplanted poly material receives no additional dose. Whilst the sheet resistivity for the metal layer could also be evaluated by using a Van der Pauw resistor structure, it is expected to be too low for an accurate measurement using the instruments available. A schematic diagram for the Van der Pauw resistor structure is shown below:

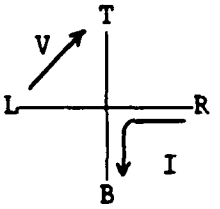



where "NT", "NR", "NB" and "NL" represent the probe access pads that are connected to the top, right-hand, bottom and left-hand arms respectively of the Van der Pauw resistor structure evaluated by procedure VDP.

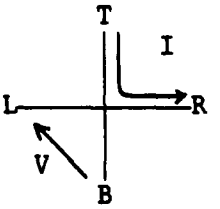
This structure provides a direct measurement of the sheet resistivity of the central square, defined by the intersection of the two perpendicular tracks. There are four terminal-configurations of interest. When current is forced between any pair of adjacent arms, a voltage will be developed between the other two arms, which is expected to be a linear function of the current actually flowing. If the Van der Pauw structure is perfectly symmetrical and is delineated in uniformly conductive material, then the four 4-terminal resistance values obtained would all be equal. The sheet resistivity is obtained by multiplying the resistance value by pye, then dividing the result by the natural logarithm of two.

The four terminal-configurations possible can be grouped into two pairs, where the input and output ports for the terminal-configurations in each pair have been transposed. This is shown below:

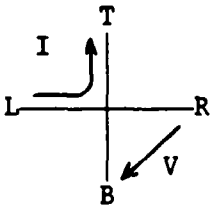
Configuration 1



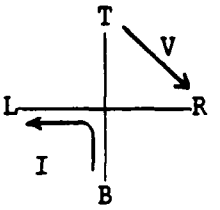

Configuration 2




Configuration 3




Configuration 4




Configurations 1 and 3 are expected to exhibit reciprocity. This pair is denoted as "pair #1". Similarly, configurations 2 and 4 are expected to exhibit reciprocity. This pair is denoted as "pair #2".

The two 4-terminal resistance values obtained for each pair are averaged and used to calculate the sheet resistivity value implied. A reciprocity factor is also calculated for each pair. This is defined as the absolute value of the difference between the 4-terminal resistance values divided by the average value. The reciprocity factor value serves as the quality factor associated with the corresponding sheet resistivity value. Whilst the structure is designed to be symmetrical, the two values obtained for the sheet resistivity need not agree. The difference is primarily due to asymmetry in the electrical properties of the material since the Van der Pauw structures are tolerant to the relatively small amount of asymmetry in their geometries caused by imperfect pattern transfer. The two values for the sheet resistivity of the conductive sheet are averaged to give a single measure of this property. An asymmetry factor is also calculated. It is defined as the difference between the two sheet resistivity values obtained, divided by their average value. This average sheet resistivity value corresponds to the value implied by taking the average of all four 4-terminal resistance values. The asymmetry factor serves as the quality factor associated with this sheet resistivity value.

The measurement of the sheet resistivity of a semiconductor layer from a Van der Pauw resistor structure is based on a conductive sheet analogue, on the premise that the conductivity of the semiconductor layer involved remains unaffected by the existence of "sidewalls" along the edge of the arms defined. In practice, it is possible that the conductivity of these "sidewalls" may differ significantly from the conductivity of the "body" ( i.e. the remainder of the structure ). This has little effect when the conductivity of the "sidewalls" is less than that of the "body", because it merely reduces the effective width of the arms. Unfortunately, if the conductivity of the "sidewalls" is considerably greater than that of the

"body" ( such that current flows preferentially along the "sidewalls" ), a serious error in sheet resistivity value obtained will occur. However, the existence of preferential current paths along the "sidewalls" can be detected, by considering the ratio of the 2-terminal resistance measured between opposite arms to that measured between adjacent arms. The effect of any asymmetry can be minimised by using the average of the 2-terminal resistance values for both pairs of opposite arms and the average of the 2-terminal resistance values for all four pairs of adjacent arms. If the resistances due to the contacts involved can be neglected, these average values are expected to be in the ratio 4:3 when current flows only along the "sidewalls" and in the ratio 1:1 if there is no preferential current flow. Unfortunately, this ratio also tends to unity when the resistances due to the contacts dominate ( because both average values tend to twice the average resistance due to the contacts ). Consequently, VDP performs the additional measurements needed to calculate this ratio, but does not attempt to make any judgement on this basis. This is left to an off-line task if necessary.

The sequence of operations performed by procedure VDP is as follows. R2V is called to measure the 2-terminal resistances between the two pairs of opposite arms. The 4-terminal resistance value is measured for all four configurations, as required, by successive calls to R4V. Since R4V would come to grief if the 2-terminal resistance, measured between the voltage sensing terminals, is excessive and R4V needs a value for the 2-terminal resistance, measured between the current forcing terminals, these values are obtained by successive calls to R2V, before R4V is called. If either of these resistances exceeds one megohm, default values are assigned to both the 4-terminal resistance sought and the quality factor associated with it instead.

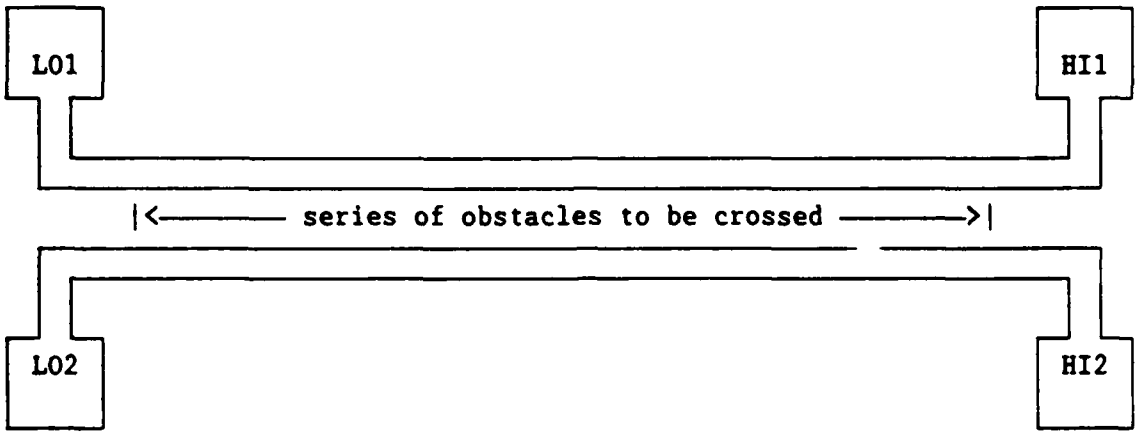
Having obtained the 4-terminal resistance values required, VDP evaluates the sheet resistivity values defined and the quality factors associated with them. If this is not possible, default values are assigned instead.

VDP also maintains encoded status words, which are associated with these three sheet resistivity values. If it is not possible to evaluate either the sheet resistivity value or its corresponding quality factor, default values are assigned instead. Bit 15 of the corresponding encoded status word is set if default values are assigned whilst the remaining bits are used to flag the reason why it was necessary to do so.

3.2.7) Step coverage check measurement procedure

Procedure SCC is called to evaluate Step Coverage Check structures. Each structure consists of a pair of parallel tracks, which cross a series of "steps" designed to provoke step coverage related problems. The problems anticipated are due to variation in the thickness of the overlying layer in the vicinity of these "steps". The existence of the "steps" may cause fractures in the overlying layer, which result in discontinuities in the pair of parallel tracks subsequently delineated. Alternatively, they may cause a localised increase in the thickness of the overlying layer which can result in the failure to remove all of the material between the pair of parallel tracks ( unless the layer is over etched sufficiently ). The resultant fillets of material form unintended "bridges" between the pair of parallel tracks defined. Step Coverage Check structures are provided to provoke and detect step coverage related problems, when the overlying layer is metal, and the "steps" are defined in either the epi layer, the poly layer or the flow glass. These "steps" are representative of those normally crossed by metal tracks. The metal tracks for the two remaining

structures are delineated on a planar surface. Two additional structures are provided using poly as the overlying layer. One structure routes the pair of parallel poly tracks over a series of "steps" defined in the epi layer ( they are the only kind of "step" normally crossed by poly ), the other routes them over a planar surface instead. A schematic diagram for the Step Coverage Check structure is shown below:



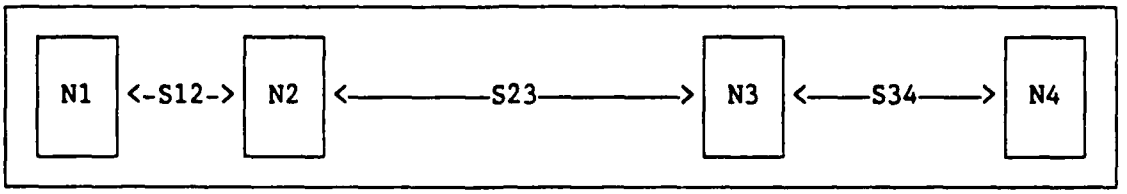

where "LO1" and "HI1" represent the probe access pads that are connected to track number 1 whilst "LO2" and "HI2" represent the probe access pads that are connected to track number 2.

The two tracks cross a series of obstacles as they traverse from left to right. They actually meander to and fro, in order to increase the number of times that they cross the obstacles. The key factors are the width of the tracks and their separation. Narrow tracks are more likely to suffer "breaks" due to step coverage problems whilst a small separation between them is more likely to result in the incomplete removal of material near to the edges of the obstacles. Thus, SCC performs a continuity test for each track and then performs isolation tests between the LO ends and the HI ends of the tracks respectively. The continuity test is performed by calling R2V, specifying a target voltage magnitude of 100mV subject to a power limit of 10mW. This ensures that the V/I source employed by R2V is able to operate in its voltage source mode for any load greater than one ohm. The isolation test is performed by calling R2V, specifying a target voltage magnitude of 10V subject to a power limit of 1mW. The relatively large target voltage magnitude specified ensures that the extremely high resistance anticipated can be measured quickly. The relatively low power limit specified is intended to reduce the probability that the "fillets" of material responsible for isolation failure will be vapourised.

3.2.8) Transmission line tapped resistor measurement procedure

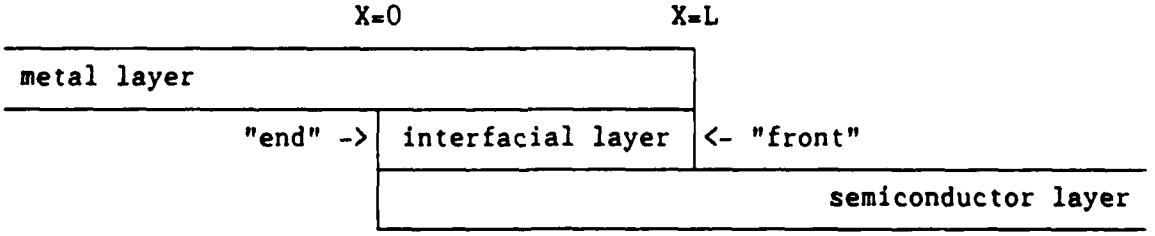
Procedure BERGER is called to evaluate Transmission Line Tapped Resistor structures. These TLTR structures consist of a rectangular strip defined in a layer of semiconductor material with four contacts formed along its length such that the nominal separation between the front edges for each pair of adjacent contacts is varied. If these contacts are identical and the separation between the front edges of each pair of adjacent contacts is known, then it is possible to discriminate between the resistance due to the contacts involved and the resistance due to the ( varied ) length of the strip of semiconductor material between them. TLTR structures are

provided to evaluate the resistance due to contacts formed to N+ epi, P+ epi and unimplanted poly respectively. These contacts are representative of the contacts used in devices realised elsewhere within the test chip. N+ epi and P+ epi receive the N and P channel source/drain implant doses respectively, whilst unimplanted poly receives neither dose. A schematic diagram of the TLTR structure is shown below:




where "N1", "N2", "N3" and "N4" represent the four contacts to the semiconductor strip ( the metal layer has been omitted for clarity ) and the separations between the "front" edges for each pair of adjacent contacts are denoted as "S12", "S23" and "S34" respectively.

If the width of the contacts and the width of the strip of semiconductor material are equal, then the Transmission Line Model for planar contacts can be exploited. Current flows between the semiconductor layer and the metal layer via an interfacial layer of indeterminate composition, which is characterised by its specific contact resistivity. The local current density within the interfacial layer is then determined by the potential difference between its upper and lower boundaries. The Transmission Line Model describes a planar contact in terms of the equivalent transmission line. For the idealised case considered, the current density within the interfacial layer varies along the length of the contact, although it is constant over the entire width of the contact. Thus, the current density is greatest at the "front" and least at the "end", as shown below:




where the thickness of the metal layer, the thickness of the interfacial layer and the thickness of the semiconductor layer have been exaggerated for clarity.

Because its sheet resistivity is extremely small, the metal layer can be considered to be an equipotential surface along the entire length of the contact. The front resistance of the contact is defined as the potential in the semiconductor layer at X=L ( with respect to the equipotential in the metal layer ) divided by the total current flowing through it. Using the equations for the equivalent transmission line, the front resistance of the contact is given by the equation:

$$RF = RSHEET * ( Lt / W ) * \coth( L / Lt )$$

where: RSHEET is the sheet resistivity of the semiconductor layer

L and W are the length and width of the contact respectively

and: Lt is the "transfer length" for the contact

This transfer length is equal to the square root of the specific contact resistivity divided by the sheet resistivity of the semiconductor layer:

i.e. Lt = sqrt( RHO(C) / RSHEET )

where: RHO(C) is the specific contact resistivity

and: RSHEET is the sheet resistivity of the semiconductor layer

It is evident that the transfer length is required to be minimised. This necessitates the minimisation of the specific contact resistivity value.

Referring to the schematic diagram for the TLTR structure, it is evident that the total resistance for any path where a current flows through the strip of semiconductor material via a pair of adjacent ( and identical ) contacts is given by:

R(path) = 2 * RF + S * RU

where: RF is the front resistance of the contacts, assumed to be equal

RU is the resistance per unit length of the semiconductor strip

and: S is the separation between the front edges of the two contacts

Thus, RF and RU could be determined from the least squares straight line fit for the measured resistance values versus the separation between the pair of contacts involved. Although the distances between the centres of each pair of contacts is known, the separation between their front edges has to be assumed to be equal to these values less the average length of the two contacts involved. If the lengths of the contacts are less than their nominal value by some fixed amount, then the front resistance will include a contribution due to the additional length of the semiconductor strip involved. Consequently, the front resistance value obtained from a TLTR structure will be in error unless the contact dimensions are known. Unfortunately, the width of the contacts is required to be less than the width of the semiconductor strip in order to accomodate any misalignment of the contact holes to the underlying semiconductor strip. This results in a 2-dimensional current distribution which invalidates the assumption made in the Transmission Line Model. The apparent front resistance value determined from a TLTR structure differs from the true value. Although a correction can be applied, this requires correction curves obtained from a rigorous simulation of the 2-dimensional current distribution.

A serious error was made when these structures were designed. In seeking to economise in the number of probe access pads necessary, the customary Kelvin connection to the metal layer, close to the contact, was omitted. Thus, the resistances due to the probe itself, the point contact between the probe tip and the probe access pad and the metal track necessary all contribute to the apparent front resistance value. Although this is not serious if the front resistance is large, it becomes the limiting factor

when the front resistance values is small ( as intended ). These errors are particularly unwelcome, because the resistance due the point contact between the probe tip and the probe access pad will vary. This variation is superimposed upon the actual variation observed across the wafer.

Procedure BERGER measures the 2-terminal resistance values for all three paths for which current flows through the semiconductor strip via a pair of adjacent contacts by making successive calls to R2V. If valid results are obtained for all three paths, then a least squares straight line fit is performed for the 2-terminal resistance values against the separation between the front edges of the corresponding pairs of contacts. Both the resistance due to each contact and the resistance per unit length of the strip of semiconductor material are calculated from the coefficients of this straight line, assuming that the contacts are all identical. BERGER also evaluates the linear correlation coefficient for the straight line. It serves as the quality factor returned for both parameters. An encoded status word is also returned for each parameter. They report the number of valid 2-terminal resistance values obtained. However, if R2V fails to return a valid 2-terminal resistance value for any of the three paths, a default values is assigned for both parameters and their quality factors instead. In this case, bit 15 is set in both encoded status words.

3.2.9) Contact chain measurement procedure

Procedure CHAIN is called to investigate the reproducibility of contacts formed between metal and semiconductor material, by evaluating the total resistance exhibited by a chain of contacts connected in series. A chain of 100 contacts is provided for contacts between metal and N+ epi, metal and P+ epi and between metal and unimplanted poly. Each chain structure is adjacent to its corresponding TLTR structure ( evaluated by BERGER ). The chain structures are realised by using short metal tracks to connect fifty pairs of contacts in series, where each pair of contacts is formed to an isolated strip of semiconductor material. The dimensions for each contact and the widths of the strips of semiconductor material contacted are identical to those used in the corresponding TLTR structure although the separation between the front edges of each pair of contacts is less. Thus, if the contacts evaluated by the TLTR structure are representative of those employed in the chain structures, the total resistance expected for a chain of 100 contacts can be estimated. The ratio of the estimated resistance to the measured value could then be evaluated, to provide the measure of reproducibility sought. Unfortunately, the design of the TLTR structures does not include separate current forcing and voltage sensing terminals which are essential if the parasitic series resistances due to the probes are to be eliminated. Thus, the estimated total resistance of a chain of contacts would be excessive. Rather than produce potentially misleading information on this basis, the total resistance for the chain of contacts is measured by calling R2V and then the result is divided by the number of contacts in the chain to obtain the average resistance per contact.

Whilst CHAIN utilises R2V to measure the total resistance for a chain of contacts, it seeks to constrain this procedure so that the points on the V/I characteristic obtained correspond to a positive current value and a negative current value respectively, where their magnitudes are equal to the value specified. When CHAIN is called, the target current magnitude required and the power limit that must be honoured by R2V are specified. These values are used by CHAIN to calculate the target voltage magnitude which is to be specified when R2V is called, in order to ensure that the

current limit for the V/I source will be set equal to the target current magnitude. When R2V attempts to force the resultant programmed voltages, the V/I source will be current limited ( as intended ) provided that the total resistance exhibited by the chain of contacts is sufficiently low.

3.2.10) Module specific procedures

Each chip is visited in turn during the wafer pass ( as specified by the "map" ). All seven modules are accessed in turn, before the next chip is visited. As each module is accessed, the procedure which is specific to that module is called to evaluate all of the structures contained within it. These procedures acquire the parametric data sought from each of the structures involved by calling the appropriate procedure ( i.e. KELVIN, VDP, SCC, BERGER or CHAIN ) and also derive further parametric data from families of structures where necessary.

Module 01 contains a family of five bridge resistor structures which are defined in the metal layer. Having accessed this module, procedure M001A is called. This procedure evaluates each of the five bridge resistors in turn, by calling KELVIN, and obtains values for the sheet resistivity of the metal layer and a linewidth loss term that characterises the pattern transfer process for this layer. It specifies a target voltage magnitude of 30mV and a power limit of 100mW. These values are passed to procedure KELVIN when it is called. They are then passed to procedures R2V and R4V where they are used to determine the stimuli applied. The target voltage magnitude of 30mV is sufficient to ensure that R2V and R4V can return an accurate result, whilst minimising the power delivered to the structures during the measurements. The power limit applied by both R2V and R4V is merely intended to protect the structures, by preventing the application of potentially destructive stimuli.

Module 02 contains a family of five bridge resistor structures which are all defined in unimplanted poly. Having accessed this module, procedure M002A is called. This procedure evaluates each bridge resistor structure in turn, by calling KELVIN, and obtains values for the sheet resistivity of unimplanted poly material and the linewidth loss term for this layer. When calling KELVIN, M002A specifies a target voltage magnitude of 30mV and a power limit of 100mW. These values are passed to both R2V and R4V, where they are used to determine the stimuli applied.

Although the poly gate electrode of the devices subsequently receive the appropriate source/drain implant dose, there is little reason to suppose that the linewidth loss for these electrodes will be affected, since the implants do not occur until after the pattern has been delineated in the poly layer as required.

Modules 03 and 04 contain a Van der Pauw resistor structure and a family of four bridge resistor structures, all delineated in the epi layer. All the structures contained in module 03 subsequently receive the N channel source/drain implant dose, whilst all the structures contained in module 04 subsequently receive the P channel source/drain implant dose instead. Procedure M003A is called to evaluate the structures contained in module 03 and procedure M004A is called to evaluate the structures contained in module 04. M003A calls VDP to obtain the sheet resistivity of the N+ epi material from the Van der Pauw resistor structure and evaluates all four bridge resistor structures in turn, by calling KELVIN. The data obtained from the family of bridge resistors is then utilised to derive the sheet resistivity of the N+ epi material and a linewidth loss term for the epi layer. Procedure M004A is similar to M003A ( the structures contained in

these two modules differ only in that they receive different implants ). Both M003A and M004A specify a target voltage magnitude of 30mV, subject to a power limit of 100mW ( these values are passed to both R2V and R4V via VDP or KELVIN as appropriate ).

The two values obtained by M003A for the sheet resistivity of N+ epi are expected to be in close agreement because all of the structures involved rely on the validity of a conductive sheet analogue. The values obtained by M004A for the sheet resistivity of P+ epi are expected to be in close agreement also. Since the source/drain implants do not occur until after the epi pattern transfer process has been completed, the values obtained for the epi linewidth loss term, by M003A and M004A respectively, should be in close agreement provided that the edges of the pattern delineated in the epi layer are vertical.

Module 05 contains three Van der Pauw resistor structures, defined in N+ poly, P+ poly, and unimplanted poly respectively, plus two Step Coverage Check structures. The Step Coverage Check structures have been designed to provoke and detect step coverage related problems. Once module 05 has been accessed, procedure M005A is called. It evaluates each of the three Van der Pauw resistor structures in turn, by calling VDP, then evaluates the two Step Coverage Check structures, by calling SCC. When M005A calls VDP it specifies a target voltage magnitude of 30mV and a power limit of 100mW. The stimuli applied by SCC are fixed. The value obtained by M005A for the sheet resistivity of unimplanted poly material is expected to be in close agreement with that derived by M002A ( using data obtained from a family of bridge resistor structures delineated in unimplanted poly ). The sheet resistivity value obtained for N+ poly is expected to be lower than that obtained for unimplanted poly, but the sheet resistivity value obtained for P+ poly is expected to be higher.

Module 06 contains five Step Coverage Check structures. These structures are designed to provoke and detect step coverage related problems. Once this module has been accessed, procedure M006A is called. This procedure evaluates each Step Coverage Check structure by calling SCC. The stimuli applied by procedure SCC are fixed.

Module 07 contains four Transmission Line Tapped Resistor structures and four contact chain structures. Since only three different types of metal to semiconductor contacts are realised ( namely, contacts to N+ epi, P+ epi and unimplanted poly ) both the TLTR structure and the contact chain structure for contacts to unimplanted poly have been duplicated. Having accessed module 07, procedure M007A is called. This procedure evaluates the front resistance value, which characterises the contacts involved in each of the TLTR structures, by calling BERGER. A target voltage of 30mV and a power limit of 10mW are specified when calling BERGER, in order to avoid "blowing" any residual dielectric layer ( which may have been left in the contact hole ). It then evaluates each of the four contact chain structures by calling CHAIN. A target current magnitude of 1mA, subject to a power limit of 10mW, is specified when calling CHAIN.

The outcome of wafer pass A is a collection of spatially related sets of parameter values, where each parameter provides information concerning a particular attribute endowed by the whole process. The spatial variation describes the variation of these attributes across the wafer and permits the subsequent investigation of suspected cause and effect relationships by the use of scatter plot techniques etc.

## 3.3) WAFER PASS E

### 3.3.1) Introduction

This wafer pass evaluates the parameters VROOT, BETA0 and THETA for each of the devices contained in modules 15, 16, 17, 18, 19 and 20 by fitting a simple equation to a set of measured ( Vgs,Ids ) points, obtained when Vds is maintained at a constant value. Although these devices do exhibit pronounced short channel effects, they are minimal when the magnitude of Vds is small. Thus, it is assumed that the Ids versus Vgs characteristic exhibited by each of these devices can be described by the equation:

$$Ids = \frac{BETA0 * ( Vgs - VROOT ) * Vds}{1 + THETA * ( Vgs - VROOT )}$$

provided that Vgs is sufficient to ensure that strong inversion has been achieved along the entire length of the channel and the magnitude of Vds is small.

Each of the modules accessed during this wafer pass contains a family of devices. These devices differ only in that their nominal channel lengths are 1um, 2um, 3um, 4um, 5um and 10um respectively. Modules 15, 17 and 19 each contain a family of N channel devices, whose nominal channel widths are 10um, 2um and 40um respectively. Modules 16, 18 and 20 each contain a family of P channel devices instead, whose nominal channel widths are also 10um, 2um and 40um respectively.

The values of VROOT, BETA0 and THETA obtained from the family of devices contained in each module are expected to be length dependent. Additional parameters are evaluated on the assumption that the length dependence of VROOT, BETA0 and THETA can each be described by simple linear equations.

The length dependence of BETA0 is assumed to be of the form:

BETA0 = BETA01 / ( Lnom - DELTAL )

where: BETA01 is the value of BETA0 for a 1um long device

and: DELTAL is the "channel length reduction" term

The length dependence of VROOT is assumed to be of the form:

VROOT = VRTINF - DELTAV / ( Lnom - DELTAL )

where: VROOT tends to VRTINF in the limit as L tends to infinity

and: DELTAV reflects the sensitivity to charge sharing effects

The length dependence of THETA is described by the equation:

THETA = THETAS + RTOTAL * BETA0

where: THETAS is the transverse electric field coefficient

and: RTOTAL is the sum of the source and drain resistances

3.3.2) Determining VROOT, BETA0 and THETA

The value of VROOT is determined by extrapolating a straight line fitted to the steepest part of the Ids versus Vgs characteristic. This value of VROOT is then utilised to derive both BETA0 and THETA, by exploiting the relationship:

$$RDS = ( THETA + RCP ) / BETA0$$

where: $RDS = ( Vds / Ids )$

and: $RCP = 1 / ( Vgs - VROOT )$

This linear relationship is expected to be applicable to all ( Vgs,Ids ) points obtained where the gate bias applied is sufficient to ensure that strong inversion occurred along the entire length of the channel. Hence, BETA0 and THETA can be obtained from the coefficients of a least squares straight line fit to RDS versus RCP for all ( Vgs,Ids ) points where the magnitude of ( Vgs - VROOT ) exceeds the minimum value needed to ensure that strong inversion occurs along the entire length of the channel. The linear correlation coefficient obtained for the least squares fit serves as the quality factor for VROOT, BETA0 and THETA.

Procedure VROOTN acquires a series of ( Vgs,Ids ) points by sweeping the bias applied to the gate whilst maintaining a constant drain bias value. The gate bias is swept so that the magnitude of the drain current should decrease progressively. Whilst the sweep is in progress, a least squares straight line is fitted to the last five ( Vgs,Ids ) points acquired and the coefficients for the straight line that exhibited the steepest slope are noted for future use. Once the slope of the latest straight line fit falls below half of the largest value found to date, the gate bias sweep is terminated on the premise that the device must have become saturated. This ensures that ample data is acquired when the device is operating in its triode region and there is no need to perform many low level current measurements ( which are relatively slow ).

The instruments are configured such that the source and the voltmeter LO are connected to ground, the gate and the voltmeter HI are connected to one V/I source, the drain is connected to the current meter HI terminal, whilst the current meter LO terminal is connected to another V/I source. Both V/I sources are programmed to operate in their voltage source mode. The current limit for the V/I source that provides the drain bias is set at 10mA. This is ample to ensure that it does not become current limited ( unless the device is defective ). The current limit for the V/I source which provides the gate bias is set at 10uA. This limit is intentionally set at a low value so that excessive gate leakage current can be readily detected ( the gate bias actually applied becomes "pinned" ).

The ( Vgs,Ids ) points required are obtained by applying the drain bias voltage specified then sweeping the gate bias voltage at equal intervals over the specified range and measuring both the voltage actually applied to the gate and the current that flows into the drain for each gate bias value programmed. The step interval used during this sweep is determined by the initial Vgs value, the final Vgs value and the maximum number of points specified. As the sweep progresses, a least squares straight line fit is performed for the five most recently measured ( Vgs,Ids ) points. If the slope of this straight line exceeds the largest value obtained to date, the coefficients of the steepest straight line fitted to date, AOS

and A1S, are updated ( they are initially assigned a value of zero ). If the latest slope value is less than 50% of the largest value obtained to date ( A1S ) the gate bias sweep is terminated. Otherwise, the gate bias will be swept over the entire range of gate bias values specified.

On completing the gate bias sweep, VROOTN uses the coefficients obtained for a straight line fitted to the steepest portion of the Ids versus Vgs characteristic ( A0S and A1S ) to estimate VROOT and BETA0 as follows:

VROOT = ( - A0S / A1S )

and: BETA0 = A1S / Vds

where the straight line fitted to the steepest portion of the Ids versus Vgs characteristic is given by:

Ids = A0S + A1S * Vgs

This is tantamount to assuming that the steepest straight line fitted to the Ids versus Vgs characteristic corresponds to the characteristic that would be exhibited by the device in the limit as THETA tends to zero.

The value of VROOT thus estimated is assumed to be sufficiently accurate to allow more accurate values of BETA0 and THETA ( i.e. non-zero ) to be derived from the coefficients of the least squares straight line fit for RDS versus RCP, as described. Because an error in the estimated value of VROOT will cause the RDS versus RCP characteristic to be non-linear, the linear correlation coefficient for the least squares fit will reveal any gross error in VROOT.

When fitting a least squares straight line to the (RCP,RDS) data derived from the measured (Vgs,Ids) points, it is imperative to exclude all data which was measured when the gate bias applied was insufficient to ensure that strong inversion occurred along the entire length of the channel.

The "effective gate bias", Vgs(eff) is defined as:

Vgs(eff) = CPOL * ( Vgs - VROOT )

where: CPOL is set equal to +1.0 for N channel devices

and: CPOL is set equal to -1.0 for P channel devices

When this "effective gate bias" exceeds the minimum value specified, the gate bias is assumed to be sufficient to guarantee that strong inversion was achieved along the entire length of the channel. This minimum value is specified to be quite large, typically ten times the value of Vds, on the assumption that it is better to reject a few "good" (RCP,RDS) points unnecessarily than to risk including a "bad" point.

Thus, VROOTN calculates the values of RCP and RDS for all (Vgs,Ids) data that meets the above criterion, then performs the least squares straight line fit for RDS versus RCP as required. The uncertainty for each of the points included in this least squares straight line fit is assumed to be proportional to the value of RDS. This causes the mean square percentage deviation to be minimised, which is consistent with the expectation that the accuracy of the RDS values are similar in percentage terms.

The straight line fitted to RDS versus RCP is described by the equation:

RDS = A0F + A1F * RCP

Thus: BETA0 = 1.0 / A1F

and: THETA = A0F / A1F

This value of BETA0 is denoted as BETAF, so that it can be distinguished from the estimated value of BETA0 ( denoted as BETAE ) obtained earlier. The linear correlation coefficient calculated for this least squares fit is used as the quality factor associated with the parameters obtained by VROOTN ( i.e. VROOT, BETAE, BETAF and THETA ). Ideally, the magnitude of the linear correlation coefficient should be unity and is expected to be positive for N channel devices and negative for P channel devices.

3.3.3) Detecting defective devices

Whilst VROOTN does not perform any preliminary measurements to check the integrity of the device currently being evaluated, a number of tests are performed which are designed to detect defect-related effects. If VROOTN identifies such an effect, it terminates the gate bias sweep and returns default values for the parameters and the quality factor associated with them. In addition, VROOTN maintains an encoded status word which is also common to all four parameters. Bit 15 of this encoded status word is set when VROOTN returns default parameter values. The remaining bits of this word are used to indicate why this action was taken.

The most likely causes of odd device characteristics are: short-circuits between the gate electrode and the source or the drain, open-circuits in the path between the probes utilised to access the source and drain, and open-circuits in the path between the probe utilised to access the gate and the gate electrode itself.

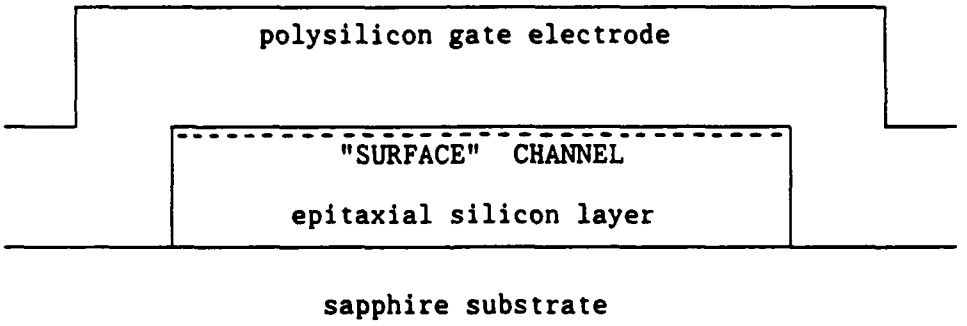
When the gate electrode is shorted to either the source or the drain, it will become pinned at a fixed potential, since the current limit for the V/I source which provides the gate bias is deliberately set such that it is unable to control the gate potential in the event of a short-circuit. The existence of such a short-circuit manifests itself when VROOTN tries to perform a least squares straight line fit for the five, most recently acquired, (Vgs,Ids) points. The coefficients of the straight line fitted share a common denominator term which depends only upon the measured Vgs values. Since the interval between successive gate bias values is known, the anticipated value of the common denominator can be calculated before commencing the gate bias sweep. When the gate bias voltage can be varied as intended, the values obtained for this common denominator term do not differ significantly from the value anticipated. However, when the gate electrode is pinned at a fixed potential, the calculated values for this term will tend to zero. Consequently, VROOTN checks the calculated value of the common denominator term for each group of five ( Vgs,Ids ) points considered and terminates the gate bias sweep if it is less than half of the value anticipated.

The Ids versus Vgs characteristic exhibited by the device is essentially flat when the drain current is not gate-controlled. Although this effect can be identified by the lack of any significant change in drain current between the extremes of the gate bias sweep, no attempt is made to check the integrity of the device on this basis. However, the slope of the Ids versus Vgs characteristic will always be positive when the drain current

is gate-controlled. Thus, VROOTN assumes that the device is defective if a negative slope value is obtained during the gate bias sweep. This test is most effective if the current flowing from the drain to the source is small because the leakage current from the gate to the drain will result in an initial slope value that is negative. Thus, open-circuits between the source and drain can be reliably detected. However, this test cannot reliably detect the existence of open-circuits between the probe used to access the gate and the gate electrode itself. This is because the drain current is often dominated by the current flowing between the drain and source of the device ( i.e. the variation in the leakage current between the gate and the drain is not detectable ). In this situation, the value of BETAE obtained is unrealistically small, since the drain current does not vary significantly with gate bias, whilst the magnitude of the value obtained for VROOT is extremely large. Consequently, VROOTN assumes that the device must be defective if the value of VROOT obtained does not lie between the specified limits for the gate bias sweep.

3.3.4) The effect of parasitic devices

Up to this point, it has been assumed that Ids is entirely due to charge transport via a "surface" channel which is formed by biasing the gate so that an inversion layer is formed in a horizontal plane, adjacent to the interface between the gate oxide and the underlying epitaxial silicon as shown below:




The above corresponds to a section through the device at right angles to the direction of current flow ( the thin gate oxide has been omitted for clarity ).

However, it is possible that the band-bending that occurs at the silicon to sapphire interface may be sufficient to result in the formation of an inversion layer, populated by free electrons, adjacent to the interface. This inversion layer forms a parasitic "back" channel between the source and drain of the N channel devices. The current that would flow via this "back" channel is expected to be largely independent of the bias applied to the gate. Whilst the process schedule includes an implant designed to to suppress the formation of a parasitic "back" channel, there can be no guarantee that it will always achieve the effect intended.

Since current can flow between the source and drain due to the transport of carriers via parasitic "sidewall" channels, adjacent to the interface between the gate oxide and the vertical edges of the active area defined by the epitaxial silicon island, the gate electrodes are always extended so that the local potential within the "sidewall" channels is controlled by the potential applied to the gate. Whilst this does not suppress the

contribution to Ids due to the parasitic "sidewall" channels, it ensures that it is at least gate controlled. The additional contribution to Ids due to the existence of the "sidewalls" of the epitaxial silicon islands can be considered to comprise of two components. One of these components is attributed to charge transport via the "sidewall" channels alone ( as if the "surface" channel did not exist ), whilst the other is attributed to the increase in the carrier density within the "surface" channel near the sharp corners where the "sidewall" and "surface" channels meet. Both are attributed to the "sidewall" channel, even though it is not strictly correct, and the "surface" channel is considered to be edgeless.

Procedure VROOTN obtains values of the parameters VROOT, BETAO and THETA on the premise that the current flowing into the drain terminal exhibits the gate bias dependence anticipated. If this premise is reasonable, the linear correlation coefficient obtained from a least squares fit for the RDS versus RCP characteristic will be close to the ideal value. However, if the parasitic "back" channel or the parasitic "sidewall" channels are responsible for a significant proportion of the current flowing into the drain terminal, the value of the linear correlation coefficient obtained by VROOTN will deviate from the ideal value by a significant amount.

Examination of the sub-threshold characteristic of the devices evaluated to date ( using a curve tracer emulation program ) indicates that "back" channel conduction has been suppressed successfully. Because there is no reason to suppose that the "sidewall" related effects are dependent upon the width of the device, the parameter values obtained for the 40um wide families of devices should be most accurate, whilst the parameter values obtained from the 2um wide devices should be least accurate.

3.3.5) Module specific procedures

Specific procedures are provided for each of the six modules accessed in wafer pass E. They are as follows:

| Module | Family | Procedure |
|---|---|---|
| 15 | 10um wide, N channel | M015EN |
| 16 | 10um wide, P channel | M016EN |
| 17 | 2um wide, N channel | M017EN |
| 18 | 2um wide, P channel | M018EN |
| 19 | 40um wide, N channel | M019EN |
| 20 | 40um wide, P channel | M020EN |

The channel widths tabulated are the nominal values. The nominal lengths of the six devices contained in each family are 1um, 2um, 3um, 4um, 5um, and 10um respectively. These procedures call VROOTN to obtain values for parameters VROOT, BETAE, BETAF and THETA from each of the six devices in the appropriate module. For N channel devices, they specify a drain bias of +100mV and a gate bias "sweep" from +5.0V to -5.0V in 0.1V steps. For P channel devices, both the polarity of the drain bias and the direction of the gate bias sweep are reversed.

Because VROOTN "sweeps" the gate bias so that the magnitude of the drain current should decrease as the "sweep" progresses and terminates it once the device has become saturated, the initial gate bias value is required to be sufficient to ensure that an adequate number of ( Vgs,Ids ) points can be obtained during the "sweep" whilst the final gate bias value must

be sufficient to ensure that the device will become saturated before the "sweep" is completed. Thus, by allowing the gate bias to be "swept" over the widest range permissible, VROOTN can accomodate VROOT values over as wide a range as possible.

These procedures also specify a minimum "effective gate bias" magnitude, which is utilised to select the ( Vgs,Ids ) points to be included in the least squares straight line fit to the RDS versus RCP characteristic. It is specified to be 1.0V for all devices, regardless of their dimensions. This value is sufficient to guarantee that all of the ( Vgs,Ids ) points included were obtained when the device in question was biased so that it was operating in its triode region. Although the minimum "effective gate bias" magnitude specified is slightly excessive, it ensures that a small error in the value obtained for VROOT can be tolerated. Since the effect of excluding a few ( Vgs,Ids ) points unnecessarily upon the accuracy of the values obtained for BETAF and THETA is minimal, a slightly excessive minimum "effective gate bias" magnitude is less likely to result in poor accuracy than a value which is too small.

Once parameters VROOT, BETAE, BETAF and THETA have been evaluated, these procedures evaluate three additional pairs of parameters, which describe the length dependence of VROOT, BETAF and THETA repectively. Whilst they log the values of all four parameters obtained by VROOTN, the values of BETAE are logged merely to reveal the inadequacy of the assumptions made when using the steepest portion of the Ids versus Vgs characteristic for the device in question to evaluate BETA0.

The three additional pairs of parameters sought are evaluated by calling a procedure which is common to all six module specific procedures. This procedure performs three least squares straight line fits in turn, which yield values of the parameters DELTAL and BETAF1, VRTINF and DELTAV, and THETA and RTOTAL respectively.

The first least squares straight line fit performed assumes that:

$$( 1 / BETAF ) = ( Lnom - DELTAL ) / BETAF1$$

where: DELTAL is the "channel length reduction" term

and: BETAF1 is the value of BETAF for a 1um long device

By fitting a least squares straight line to 1/BETAF versus Lnom, for all devices whose BETAF values could be obtained, both DELTAL and BETAF1 can be evaluated.

If the least squares straight line fit can be performed and the straight line thus fitted is described by the equation:

$$( 1 / BETAF ) = A0 + A1 * Lnom$$

then the values of DELTAL and BETAF1 can be obtained, since:

$$DELTAL = ( - A0 / A1 ) \quad \text{and} \quad BETAF1 = ( 1 / A1 )$$

The linear correlation coefficient calculated for this least squares fit serves as the quality factor associated with both DELTAL and BETAF1. The encoded status words associated with these parameters are both set equal to the number of devices whose BETAF values were excluded from the least squares straight line fit ( because VROOTN assigned a default value ).

If there are fewer than three non-default values of BETAF available, the least squares straight line fit, required to evaluate DELTAL and BETAF1, cannot be performed. In this event, both parameters are assigned default values instead. The quality factors associated with these parameters are also assigned default values and bit 15 of their encoded status words is set to indicate that default values have been assigned.

The second least squares straight line fit performed assumes that:

$$Leff = ( Lnom - DELTAL )$$

and: $VROOT = VRTINF - DELTAV / Leff$

where: Leff is the effective length of the channel

VROOT tends to VRTINF in the limit as Leff tends to infinity

and: DELTAV reflects the sensitivity to charge sharing effects

Before the least squares fit can be performed, it is necessary to set-up arrays which contain the values of VROOT obtained and the reciprocals of Leff for the corresponding devices. Entries are made in the arrays only if a non-default value was assigned to VROOT for the device in question, and the calculated value of Leff is positive, non-zero. Evidently, it is impossible to calculate the effective channel length values if a default value has been assigned to DELTAL and it is only possible to perform the least squares straight line fit if at least three entries have been made in these arrays.

If the least squares straight line fit can be performed and the straight line thus fitted is described by the equation:

$$VROOT = A0 + A1 * ( 1 / Leff )$$

the values of VRTINF and DELTAV can be calculated, since:

$$VRTINF = A0 \quad \text{and} \quad DELTAV = ( - A1 )$$

The linear correlation coefficient calculated for this least squares fit serves as the quality factor associated with both VRTINF and DELTAV. The encoded status words associated with these parameters are both set equal to the number of devices for which it was not possible to obtain a point on the VROOT versus 1/Leff characteristic.

When a least squares straight line fit for VROOT versus 1/Leff cannot be performed, VRTINF and DELTAV can not be evaluated. In this case, default values are assigned to both parameters instead. Default values are also assigned to the quality factors associated with these parameters and bit 15 of their encoded status words is set to indicate that default values have been assigned.

The third least squares fit performed assumes that:

$$THETA = THETAS + RTOTAL * BETAF$$

where: THETAS is the transverse electric field coefficient

and: RTOTAL is the sum of the source and drain resistances

Both THETAS and RTOTAL can be derived from the coefficients of the least squares straight line fitted to THETA versus BETAF for all devices where non-default values of these parameters were obtained.

If the least squares straight line fit can be performed and the straight line thus fitted is described by the equation:

THETA = A0 + A1 * BETAF

then the values of THETAS and RTOTAL can be obtained, since:

THETAS = A0 and RTOTAL = A1

The linear correlation coefficient calculated for this least squares fit serves as the quality factor associated with both THETAS and RTOTAL. The encoded status words associated with these parameters are both set equal to the number of devices whose THETA and BETAF values were excluded from the least squares straight line fit.

If fewer than three non-default values of THETA and BETAF are available, then the least squares straight line fit required to evaluate THETAS and RTOTAL can not be performed. In this event, both parameters are assigned default values instead. Default values are also assigned to the quality factors associated with these parameters. Bit 15 of their encoded status words is set when default values have been assigned.

Each of the module specific procedures called during wafer pass E record the parameter values obtained plus the quality factor and encoded status word values associated with them in the "log" file created. This data is prefixed by the set of "key strings" assigned by the operator before the wafer pass was commenced.

## 3.4) WAFER PASS F

### 3.4.1) Introduction

This wafer pass performs a similar function to wafer pass E, except that it uses a different method to evaluate parameters VROOT, BETA0 and THETA for each of the devices accessed during the wafer pass. These parameters are evaluated for the families of six devices contained in modules 15 to 20 inclusive. The additional parameters necessary to describe the length dependences of VROOT, BETA0 and THETA are also evaluated for each module using the same method as that employed in wafer pass E. Since the values of VROOT, BETA0 and THETA are evaluated by using a different method, the values assigned to these parameters will be slightly different.

The method employed to evaluate parameters VROOT, BETA0 and THETA during this wafer pass is based upon that described for wafer pass E. Whilst it utilises the same methods to acquire the ( Vgs,Ids ) points required and estimate VROOT, it does not assume that this value is accurate. Instead, the value of VROOT is adjusted in order to achieve the best fit possible to the linear RDS versus RCP characteristic anticipated. Once an optimum value of VROOT has been obtained, the values of BETA0 and THETA are then calculated from the coefficients of a least squares straight line fitted to the RDS versus RCP characteristic obtained when VROOT is set equal to its optimum value. The values of VROOT, BETA0 and THETA obtained by this method are believed to be more accurate than those obtained during wafer pass E since the linear correlation coefficients obtained for this least squares straight line fit are consistently closer to their ideal value. Consequently, the values of the parameters used to describe their length dependences should also be more accurate.

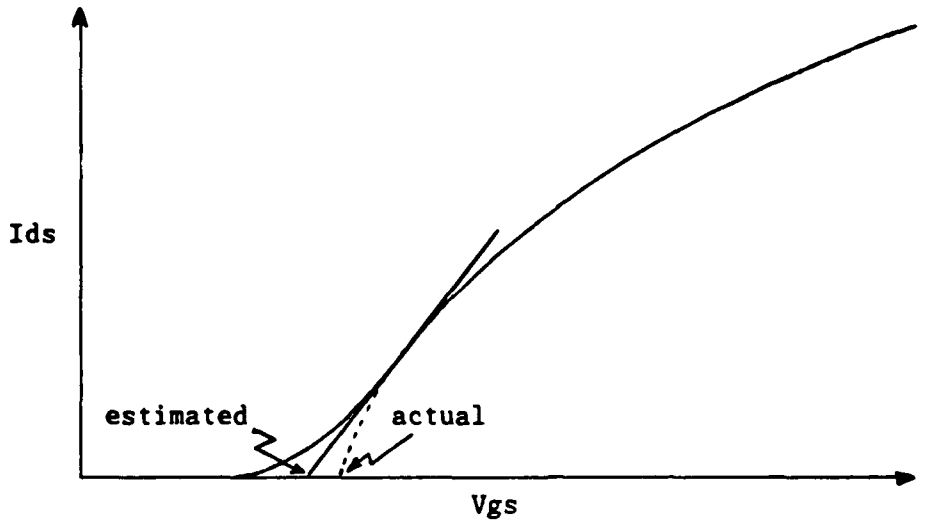
Despite the improvement in the accuracy of the parameter values obtained during wafer pass F, the method used to evaluate parameters VROOT, BETA0 and THETA tends to conceal the effects of any additional contribution to Ids due to the existence of a parasitic "back" channel and those effects attributed to the "sidewalls". Another area of concern is the robustness of the complicated algorithm employed to optimise VROOT, although it has not failed to date. Consequently, wafer pass F is ( currently ) regarded as an alternative to wafer pass E rather than its successor.

The procedure employed to evaluate the parameters VROOT, BETA0 and THETA acquires the set of ( Vgs,Ids ) points required, then estimates VROOT by extrapolating the steepest portion of the Ids versus Vgs characteristic. This estimated value of VROOT is expected to be offset slightly from the optimum value, since the Ids versus Vgs characteristics exhibited by the devices will deviate from that predicted by the equation:

$$Ids = \frac{BETA0 * ( Vgs - VROOT ) * Vds}{1 + THETA * ( Vgs - VROOT )}$$

as Vgs approaches VROOT because the device becomes saturated. The offset is due to the failure to account for the curvature of the above equation between the value of Vgs where the steepest slope is observed and VROOT. Whilst this offset is small, it is sufficient to result in non-linearity of the RDS versus RCP characteristic. This can be minimised by making an appropriate adjustment to the value assigned to VROOT.

The error in the value of VROOT estimated by extrapolating the steepest portion of the Ids versus Vgs characteristic is shown below:




3.4.2) Optimising VROOT, BETAO and THETA

In order to adjust the value of VROOT, so that the best fit possible can be achieved, it is necessary to utilise a measure of the accuracy of the fit. Whilst the deviation of the linear correlation coefficient from its ideal value could provide such a measure, it is subsequently used as the quality factor associated with parameters VROOT, BETAO and THETA. Hence, an alternative "target" ( which is to be minimised ) is employed.

The coefficients of the straight line fitted by the least squares method are such that the sum of the squares of the deviations from the straight line thus fitted, for all points included in the fit, will be minimised. The reduced chi squared term is defined to be equal to this sum, divided by the number of points included, less the number of degrees of freedom. The method used to optimise the value of VROOT exploits the observation that the reduced chi squared term obtained for a least squares straight line fit to the RDS versus RCP characteristic can be minimised by making the appropriate adjustment to the value of VROOT. Therefore, the reduced chi squared term is used as the "target" function to be minimised.

Denoting the adjustment made to the estimated value of VROOT as ADJ, and the corresponding value of the reduced chi squared term as CHI, then the CHI versus ADJ characteristic invariably exhibits a well-defined minimum which indicates that an optimum value of ADJ exists. This characteristic is approximately quadratic when ADJ is close to its optimum value.

The optimisation algorithm employed finds the value of ADJ, necessary to minimise CHI, within the range of ADJ values specified. The range of ADJ values permitted is defined by the calling procedure which specifies the maximum magnitude of ADJ allowed. Before the CHI versus ADJ function can be investigated, it is necessary to select the set of ( Vgs,Ids ) points subsequently used to perform the least squares straight line fits to RDS versus RCP. The method employed is similar to that used in wafer pass E. That is, the "effective gate bias" is calculated for each point obtained on the Ids versus Vgs characteristic. Those points whose "effective gate bias" exceeds the minimum value specified are included in the subsequent

optimisation process. The remainder are ignored on the grounds that they may have been measured when the device in question was not operating in its triode region. The values of RDS required are calculated once only, since RDS is independent of ADJ, but the corresponding values of RCP are calculated for each value of ADJ considered.

The first task is to determine whether a well-defined minimum in the CHI versus ADJ characteristic exists within the range of ADJ values allowed. The value of CHI is determined for the upper and lower limits of ADJ and at the mid-point of the span. A well-defined minimum in CHI exists only if the middle value of ADJ corresponds to the smallest value of CHI. The three ADJ values are then said to have "straddled" the optimum value. In the unlikely event that the optimum value of VROOT is not "straddled" as expected, the procedure aborts. A default value will be assigned to both the parameters evaluated by this procedure and their quality factors, if it aborts for any reason. Bit 15 of the encoded status words associated with these parameters is set if default values have been assigned whilst the remaining bits are used to indicate why this action was necessary.

If the three values of ADJ tried by the optimiser "straddle" the optimum value, it uses quadratic interpolation to calculate the turning point in the CHI versus ADJ characteristic, denoted as ADJTP. This value of ADJTP is approximate, but becomes increasingly accurate as the span of the ADJ values utilised is progressively reduced in subsequent iterations, since the second derivative of CHI with respect to ADJ will tend to a constant value as the interval between the three ADJ values used is decreased.

In subsequent iterations, the optimisation algorithm tries three new ADJ values, centred on ADJTP. The step interval between these values is half that used previously. Hence, the optimisation algorithm closes-in on the optimum value of ADJTP in successive iterations. Evidently, this process must be terminated once the required accuracy has been achieved. This is determined by monitoring the "precision factor", which is defined as the r.m.s. deviation for the three values of CHI currently obtained, divided by their mean value. The iterative process is terminated once the value of the "precision factor" falls below the minimum value allowed. This is fixed at ten parts per million. The maximum number of iterations allowed is limited to twenty, as an additional safeguard, although the iterative process is usually terminated in less than ten iterations.

Once the value of ADJ necessary to minimise the reduced chi squared term for the least squares fit for the RDS versus RCP characteristic has been determined, the optimum value of VROOT is calculated by adding the value of ADJTP obtained in the last iteration to the value of VROOT originally estimated. This value is denoted as VRTMN.

The corresponding values for BETA0 and THETA are evaluated by performing a least squares straight line fit for the ( RCP,RDS ) points obtained by using the value assigned to VRTMN to calculate the RCP values necessary. The linear correlation coefficient calculated for this least squares fit serves as the quality factor for these parameter values.

The procedure which evaluates VRTMN, BETA0 and THETA by using the method described also returns the estimates of VROOT and BETA0 derived from the coefficients obtained for a straight line fitted to the steepest portion of the Ids versus Vgs characteristic. To avoid confusion, the estimated value of BETA0 is described as BETAE, whilst the value obtained from the least squares straight line fit is described as BETAF instead.

The five parameters that are evaluated, for each of the devices accessed during wafer pass F, are as follows:

| Parameter | Description |
|---|---|
| VROOT | the value of VROOT initially estimated |
| BETAE | the value of BETA0 initially estimated |
| VRTMN | the optimum value of VROOT ( fitted ) |
| BETAF | the optimum value of BETA0 ( fitted ) |
| THETA | the optimum value of THETA ( fitted ) |

The values obtained for VROOT and BETAE are only returned to demonstrate that the so called "steepest slope" method is decidedly inaccurate. Only VRTMN, BETAF and THETA are of any further interest.

3.4.3) Module specific procedures

Specific procedures are provided for each of the six modules accessed in wafer pass F. They are as follows:

| Module | Family | Procedure |
|---|---|---|
| 15 | 10um wide, N channel | M015FN |
| 16 | 10um wide, P channel | M016FN |
| 17 | 2um wide, N channel | M017FN |
| 18 | 2um wide, P channel | M018FN |
| 19 | 40um wide, N channel | M019FN |
| 20 | 40um wide, P channel | M020FN |

The channel widths tabulated are the nominal values. The nominal lengths of the six devices contained in each family are 1um, 2um, 3um, 4um, 5um, and 10um respectively. These procedures specify the fixed drain bias, to be applied to the device in question, the gate bias "sweep" required and the interval between successive gate bias values. For N channel devices, a fixed drain bias of +100mV and a gate bias "sweep" from +5.0V to -5.0V in 0.1V steps are specified. For P channel devices, the polarity of the drain bias and the direction of the gate bias "sweep" are both reversed. These values are identical to those specified for wafer pass E. However, it is observed that the interval between successive gate bias values can be doubled, thereby reducing the time spent performing the "sweep", with no apparent degradation in the accuracy of the parameter values obtained ( although this is not normal practice ), since the optimiser is capable of correcting for the additional error in the initial estimates of VROOT thus introduced.

These procedures also specify a minimum "effective gate bias" magnitude, which is utilised to select the ( Vgs,Ids ) points included in the least squares straight line fit performed for the corresponding RDS versus RCP characteristic. The value specified is 1.0V for all devices, regardless of their dimensions ( i.e. the same as that specified in wafer pass E ). They are also required to specify the maximum adjustment in the value of VROOT allowed whilst seeking to optimise its value. A maximum adjustment of 100mV is specified for all devices, regardless of their dimensions.

These procedures evaluate all six devices contained in the corresponding module and also perform a 2-terminal resistance measurement, between the source and drain terminals of the "zero length devices" included in each of these modules. The value of this resistance is determined by calling the procedure R2V ( see wafer pass A ) and is denoted as R(L=0). Each of these "zero length devices" are identical to the other devices contained within the module concerned in all respects other than that the width of their gate electrodes has been shrunk to zero ( i.e. the gate electrodes do not exist ). The sum of the resistance associated with the source and the resistance associated with the drain, RTOTAL, differs from R(L=0) by an amount which is attributed to the spreading resistances at the source and drain ends of the channel ( because the carriers are transported via a thin inversion layer from source to drain ). Thus, measuring the value of R(L=0) and determining RTOTAL provides valuable information regarding the relative significance of the spreading resistance contributions.

Having evaluated the family of devices and the "zero length device", the three pairs of parameters employed to describe the length dependences of VRTMN, BETAF and THETA are evaluated by performing the appropriate least squares straight line fits. This is achieved by making use of a similar procedure to that employed in wafer pass E.

Each of the module specific procedures called during wafer pass F record the parameter values obtained plus the quality factor and encoded status word values associated with them in the "log" file created. This data is prefixed by the set of "key strings" assigned by the operator before the wafer pass was commenced.

# 4.0) DATA MANAGEMENT AND ANALYSIS

## 4.1) Introduction

The parametric data acquisition programs create separate "log" files for each of the wafer passes that they perform. Each "log" file contains all of the parametric data acquired during the wafer pass plus the values of the "key strings" assigned at run-time. The structure of the "log" files has been described in the section entitled "Parametric Data Acquisition Program Structure".

The basic unit of parametric data is described as a "result", where each "result" consists of the value assigned to a particular parameter by the appropriate measurement procedure, plus the corresponding quality factor and encoded status word values. The parametric data acquisition programs record the "results" obtained from each module accessed during the wafer pass as soon as possible, in order to minimise the demands made upon the limited amount of virtual address space available. Consequently, data is stored in the "log" file in an order which is not conducive to the rapid retrieval of the set of "results" obtained for a given parameter for all chips visited during the wafer pass.

The database load utility, DBLOAD, operates upon all "log" files created since it was last run, dealing with them in chronological order. It uses the data contained in each "log" file to create a new "data" file and to construct a record which is appended to the "master" file. When creating the new "data" file, DBLOAD assembles a "result-set" for every parameter evaluated. The "result-set" for a given parameter consists of the set of "results" obtained for that parameter from every chip visited during the wafer pass. Having assembled the "result-sets", DBLOAD then writes them to consecutive "data" file records. Thus, the "data" file structure will allow the subsequent retrieval of the "result-set" sought by reading the appropriate "data" file record.

## 4.2) Database structure

The "master" file provides the means whereby the "data" file of interest can be identified. Each "master" file record contains the "key strings" read from the "log" file, the name assigned by DBLOAD to the "data" file that it created and the additional fields required for proper operation. Thus, the name of the "data" file sought can be subsequently obtained by finding the "master" file record whose "key strings" correspond to those assigned to the wafer pass of interest.

The "data" files created are sequentially organised, with direct access, which provides random access to any record within them. Any "result-set" can therefore be retrieved at will. Since each of the "results" within a given "result-set" is associated with a particular chip, the "data" file records each contain the appropriate set of "results", stored in exactly the same chip-sequential order ( this order is identical to the order in which the chips were visited ) whilst the corresponding chip coordinates are stored in the last "data" file record. The "result-sets" are written to consecutive "data" file records in a known order. That is, the set of "results" obtained for the Nth parameter evaluated at every chip visited during the wafer pass is written to the Nth "data" file record. If there are NMAX "result-sets" stored in the "data" file, the corresponding chip coordinates are written to record number ( NMAX + 1 ). Thus, the spatial relationship between the "results" contained in any of the "result-sets" can be subsequently determined by reading this record.

A separate database utility program creates a "descriptor" file for each parametric data acquisition program. The Nth record in this "descriptor" file contains a descriptive text string for the Nth "result-set" for any "data" file created as a result of running that program. These files are sequentially organised, with direct access, so that the descriptive text string for any "result-set" can be retrieved at random. The "descriptor" files created by this utility are given filenames which can be generated from the value assigned to the Test Plan "key string" by the appropriate parametric data acquisition program at run-time. Thus, the "master" file entry for the wafer pass of interest is utilised to open both the "data" file required and the corresponding "descriptor" file.

The RSX11-M file management system requires that all records in a direct access file must have the same length and that this length must be known when the file is opened. Since the record length for each "data" file is dependent upon the number of chips visited during the wafer pass, DBLOAD creates "data" files with the appropriate record length and inserts this information in the corresponding "master" file entry. DBLOAD also stores the number of chips visited during the wafer pass in this entry, because it has to append extra bytes in the "data" file records if the number of chips visited during the wafer pass is odd ( the record length specified must be a multiple of 20 bytes whilst a "result" consists of 10 bytes ). Since the programs which subsequently read the "data" files will need to know the number of "result-sets" contained within them, this information is also stored in the corresponding "master" file entry by DBLOAD. It is not necessary to store the length of the "descriptor" file records since their length is fixed at 40 bytes.

4.3) Data retrieval

A number of programs are provided to facilitate the analysis of the data obtained by [redacted] parametric data acquisition programs. These programs all operate upon the "data" file identified by the user. This is achieved by asking the user to nominate one of the "key strings" ( included in every "master" file entry ) as the "primary key" and then to specify the value of the "primary key" sought. The "master" file entries are then examined in turn and all entries where the "primary key" corresponds to the value sought are reported. The user is then asked to identify the entry which corresponds to the wafer pass of interest by examining the values of the other "key strings". The information contained within the "master" file entry identified by the user allows the programs to open the appropriate "data" file and the corresponding "descriptor" file. The number of chips visited during the wafer pass plus the number of "result-sets" contained within the "data" file are also noted for future use. The last record in the "data" file is read in order to set-up arrays which contain the chip coordinates. This information is used to define the spatial relationship between the "results" for all "result-sets" contained in the "data" file selected. The last record in the "data" files also contain the values of the pass/fail status flags, assigned by the registration check procedure for each chip visited during the wafer pass. The data analysis programs use this information to generate a wafer "map" displaying the outcome of the registration check for all chips visited during the wafer pass. This provides a useful check when the parametric data acquisition program was left to run unattended.

The data analysis programs utilise the contents of the "descriptor" file to help the user pick each of the "result-sets" of interest in turn, via a menu that is automatically generated and paginated. The user can elect to include all of the "result-sets" available in this menu or to include

only those "result-sets" where the corresponding descriptive text string contains the sub-string specified. Once the "result-set" of interest has been selected, by specifying the appropriate record number listed in the menu, it is retrieved by reading corresponding "data" file record. Since the parametric data acquisition programs assign default parameter values and default quality factors when they are unable to quantify them, it is necessary to exclude the corresponding "results" when seeking to analyse the "result-set" of interest. Two arrays of logical flags are set-up so that this can be easily accomplished. One array identifies the "results" where a default parameter value was assigned whilst the other identifies those "results" where a default quality factor value was assigned.

4.4) Data sorting

Before the "results" included in the "result-set" currently selected can be analysed, it is necessary to "sort" them in order to separate the few "results" that are dubious from the remainder. Dubious "results" usually arise when a parametric data acquisition program fails to recognise that the test structure concerned is defective and attempts to evaluate those parameters used to describe its electrical characteristics despite this. Although the parametric data acquisition programs seek to identify those test structures that are grossly defective and assign default values for both the parameter value and the corresponding quality factor, there can be no guarantee that the parameter value otherwise obtained is accurate. Consequently, the data analysis programs must include mechanisms for the exclusion of "results" which are of questionable accuracy. The principal method of discrimination is based upon examination of the quality factor values.

The parameter values obtained from a particular test structure will only be meaningful if the test structure concerned has the properties that it is expected to exhibit. The quality factor associated with each "result" will be close to the optimum value when the test structure concerned has the properties expected. This is the basis of the "sort" operations used by the data analysis programs. A histogram for the quality factor values is displayed to reveal the existence of dubious "results". Normally this histogram exhibits a tight distribution of the quality factors, close to the optimum value. The user is then given the opportunity to exclude all "results" whose quality factors differ significantly from the remainder, on the basis that "results" whose quality factors are not representative of the "result-set" as a whole are unlikely to include an accurate value for the parameter in question. The logical flags associated with each of the "results" are modified as necessary in order to achieve this end.

One particularly attractive feature of this "sorting" method is that the user only needs to know that the quality factor values should be tightly distributed. Since it is completely independent of the parameter values, "sorting" by quality factor value does not distort the statistics of the set of parameter values obtained for the "result-set" of interest.

Whilst the relatively few dubious "results" can usually be distinguished from the remainder by their unrepresentative quality factor values, this method of "sorting" is not totally effective. A few of the "results" may have a quality factor that is close to the optimum value and a parameter value that is considerably different from the remainder. These "results" are rare ( fewer than one in ten thousand ). The difficulty here is that there is no way of discriminating between "results" whose quality factor happens to be close to the optimum value and those whose parameter value genuinely differs from the remainder by a significant amount.

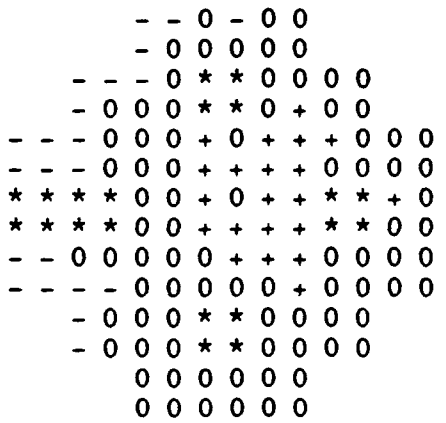
Schmoo plots are used to display the spatial variation for the parameter values. The Schmoo plot consists of an array of symbols which correspond to the chip locations the wafer. The symbol assigned to each location is determined by the parameter value for the corresponding chip. An example of the Schmoo plots generated is shown below:

Descriptor: RSHEET for "doped" polysilicon layer

Units: ohms per square

Mean parameter value: 1.85252E+01
R.M.S. deviation: 4.83309E-01
Normalised deviation: 2.60893E+00

Number of valid samples: 128



The symbols in the Schmoo plot signify the following:

| SYMBOL | SIGNIFICANCE |
|---|---|
| < | the value is less than ( MEAN - 5 * RMS ) |
| = | ( MEAN - 5 * RMS ) to ( MEAN - 3 * RMS ) |
| - | ( MEAN - 3 * RMS ) to ( MEAN - 1 * RMS ) |
| 0 | ( MEAN - 1 * RMS ) to ( MEAN + 1 * RMS ) |
| + | ( MEAN + 1 * RMS ) to ( MEAN + 3 * RMS ) |
| # | ( MEAN + 3 * RMS ) to ( MEAN + 5 * RMS ) |
| > | the value is more than ( MEAN + 5 * RMS ) |
| ? | the "result" is not considered to be valid |

Non-standard asterisks have been inserted in the Schmoo plot to indicate the grid locations on the wafer "map" which the data acquisition program concerned did not visit. These locations correspond to standard drop-ins and the area reserved for wafer identification purposes. The size of the "buckets" employed to create the Schmoo plot tracks the r.m.s. deviation for the parameter values. Thus, the symbols assigned in the Schmoo plot reveal the spatial variation of the parameter values whilst the value of

the r.m.s. deviation provides a measure of its magnitude. The values for the "normalised deviation" correspond to the r.m.s. deviation, expressed as a percentage of the mean value. Thus, this example demonstrates that the sheet resistivity for the "doped" polysilicon gate layer exhibits an r.m.s. deviation which is a mere 2.61 percent of the mean value.

This example shows a spatial variation which is fairly typical. That is, few parameter values differ from the mean value by more than three times the r.m.s. deviation, whilst "results" where the parameter value differs from the mean by more than five times the r.m.s. deviation are extremely rare.

Where the Schmoo plot includes a "result" whose parameter value deviates from the mean by more than five times the r.m.s. deviation, the user can elect to exclude it. This is justified on the premise that such a value is extremely improbable. All of the "results" excluded on this basis are indicated by the symbol 'K' ( i.e. the "result" has been "killed" ). The majority of the parameter values excluded in this manner have been found to correspond to peripheral chip locations, where it is most likely that the parameter values obtained differ significantly from the remainder.

4.5) Data analysis

The data analysis requirement is satisfied by the programs DBLOOK, DBSUM and DBSCAT. These programs are general purpose, in that they can operate upon any "data" file created by DBLOAD. Each program performs the series of data retrieval and "sorting" operations described. Whilst DBLOOK and DBSUM operate on each "result-set" selected in turn, DBSCAT requires the user to select a pair of "result-sets", then produces a scatter plot for one versus the other ( having first "sorted" each "result-set" ) so that any correlation between them can be recognised.

DBLOOK outputs a text file which contains a one page summary for each of the "result-sets" selected by the user. This summary includes the Schmoo plot generated, the minimum and maximum quality factor for all "results" ( excluding those where a default value was assigned ), the low and high quality factor limits used when "sorting" the "result-set" selected, and the number of parameter value samples that are deemed to be valid.

DBSUM satisfies the requirement for a short-form summary report. Whilst it displays the Schmoo plot generated for each "result-set" selected, in order allow the user to reject those parameter values whose deviation is in excess of five times the r.m.s. deviation when deemed necessary, this information is not included in its output text file. Instead, it merely tabulates the descriptive text string, the number of "results" deemed to be valid, the mean and the r.m.s. deviation for the corresponding set of parameter values, plus the lower and upper limits applied to the quality factor values when the "result-set" in question was "sorted".

The judicious utilisation of these programs is sufficient to ensure that no significant information need be lost. First, DBSUM is used to produce a short-form summary, noting any "result-set" whose spatial variation is unusual. DBLOOK is then used to produce a more detailed report for these "result-sets" only. DBSCAT is primarily an investigative tool.

## 5.0) CONCLUSIONS

The parametric testing methodology implemented was originally devised to address the problems anticipated when using an unproven test chip design to evaluate the outcome of an otherwise uncharacterised CMOS, silicon on sapphire process. The introduction of quality factors, which are used to independently validate the design of the structures included in the test chip and to verify the assumptions implicitly made, when formulating the generic equations used to describe their electrical characteristics, has been demonstrated to be of considerable value in practice. It eliminates the need for a separate validation exercise ( which would be specific to a particular process schedule ) and also provided the means of verifying that the assumptions originally made remain valid, as the target process evolves.

Since the measurement procedures employed adjust the stimuli applied to the structures in order to obtain the responses sought, they do not need prior knowledge of the range of parameter values anticipated. Evidently, they do rely upon the structures exhibiting the properties expected when seeking to adjust the stimulus applied, but these properties are usually substantially independent of the parameter values obtained. As a result, they can accurately evaluate the parameters sought over the widest range of values possible.

The parametric data analysis programs also avoid the necessity for prior knowledge of the range of parameter values expected by using the quality factor associated with each of the parameter values obtained to identify the structures that are likely to have yielded dubious parameter values. This approach is far more even-handed than the conventional method which excludes all parameter values that do not fall within the "valid limits" specified.

Clearly, the execution time for each parametric data acquisition program is greater than that for a minimal implementation, due to the additional measurements necessary to adjust the stimulus applied to each structure and to obtain the redundant information required to evaluate the quality factors associated with the parameter values thus obtained. However, the ability to track changes in the parameter values caused by variations in the process schedule and the built-in confidence checking resulting from the use of quality factors are well worth the additional run-time.

This methodology is particularly suitable for a research and development environment, where the limited resources available are deployed in order to improve upon the base-line process at the possible expense of process control and the wafer throughput is relatively small. Split batches can be readily supported, since all the information required can be obtained from a single wafer if necessary.

## APPENDIX 1: INDIVIDUAL MODULE DESCRIPTIONS

### Module 00, Probe to Module Pad Registration Check

This purpose of this module is to ensure that the alignment of the probe card to the wafer is sufficient to minimise the probability that useless data is obtained during a wafer pass. Evidently, it is necessary to make sure that the probes "hit" the probe access pads of the module currently being accessed by the automatic wafer prober if erroneous results are to be avoided.

The probe access pads for this module are connected to one another via a central spine defined in metal. When the probes are correctly aligned to the wafer, a low resistance path should be detected between all pairs of probes when the module is accessed. The probe access pads of this module are undersized by 5um all round. This figure corresponds to the maximum positioning error for the X,Y stage of the wafer prober employed. Having shown that the probes do "hit" the probe access pads of the registration check module, it is most unlikely that the probes will fail to "hit" the probe access pads of any module subsequently accessed on the same chip.

### Module 01, Metal Bridge Resistor Structures

This module contains five 4-terminal resistors which differ only in that they have different nominal widths. Each resistor comprises a long track of constant width whose ends are connected to the probe access pads used to force current along its length. There are two, widely spaced, voltage sensing taps used to measure the voltage dropped along a known length of track. These are connected to the voltage sensing probe access pads. The width of the voltage sensing taps should be minimal, since the existence of a voltage sensing tap results in a localised variation in the current flux along the track.

The distance between the voltage sensing taps is 1020um, measured along the centre-line of the metal track ( it is necessary to "fold" the metal track to produce a reasonably compact layout ). The widths of the tracks utilised to define these five resistors are 2um, 4um, 6um, 8um and 10um respectively. Because the voltage sensing taps are so widely separated, they can be made fairly wide without introducing a significant error due to localised variations in the current flux density. Hence, the width of the voltage sensing taps is 4um to improve the tolerance to poor pattern transfer fidelity.

It is assumed that the pattern transfer process is characterised by some constant over sizing or under sizing of the features delineated. This is expressed as a linewidth loss ( i.e. positive if undersized and negative if oversized ). In addition, it is assumed that the sheet resistivity of the metal layer is essentially constant within the area occupied by this module.

The objective is to determine the sheet resistivity of the metal and the linewidth loss for the metal pattern transfer process. This is achieved by measuring the conductance values for all five resistors and fitting a least squares straight line to the conductance values versus the nominal width for the corresponding resistor. The linear correlation coefficient calculated for the least squares straight line fitted can be utilised to check the validity of the assumptions made.

Module 02, Polysilicon Bridge Resistor Structures

This module contains five 4-terminal resistors which differ only in that they have different nominal widths. Each resistor comprises a long track of constant width whose ends are connected to the probe access pads used to force current along its length. Two voltage sensing taps are used to measure the voltage dropped along a known length of this track. They are connected to the voltage sensing probe access pads. Since these voltage sensing taps result in localised variation in the current flux along the track, their width should be minimised in order to minimise this effect. The contacts required for these structures are formed directly below the probe access pads. The contact dimensions are made as large as possible, in order to minimise their resistances.

The distance between the voltage sensing taps is 100um. The width of the tracks used for the five poly resistors are 2um, 4um, 6um, 8um and 10um respectively. The width of the voltage sensing taps is 2um, in order to ensure that these structures can tolerate a considerable linewidth loss.

It is assumed that the pattern transfer process is characterised by some constant over sizing or under sizing of the features delineated. This is expressed as a linewidth loss ( i.e. positive if undersized and negative if oversized ). In addition, it is assumed that the sheet resistivity of the poly layer is essentially constant within the area occupied by this module.

The objective is to determine both the sheet resistivity of the poly and the linewidth loss for the poly pattern transfer process. It is achieved by measuring the conductance values for all five resistors and fitting a least squares straight line to the conductance values versus the nominal width for the corresponding resistor. The linear correlation coefficient calculated for the least squares straight line fitted can be utilised to check the validity of the assumptions made.

Module 03, N+ Epi Bridge Resistor and Van der Pauw Structures

This module contains four 4-terminal resistors which differ only in that their nominal width is varied and a Van der Pauw resistor structure. The contacts required are formed directly below the probe access pads, using the largest dimensions possible in order to minimise their resistances.

The four 4-terminal resistors are similar to those employed in module 02 except that they are defined in N+ epi ( i.e. epi which has received the N channel source/drain implant ) instead of being defined in doped poly.

The distance between the voltage sensing taps is 100um. The width of the tracks used for the four N+ epi resistors are 5um, 10um, 15um and 20um respectively. The width of the voltage sensing taps employed is 2um, to ensure that these structures can tolerate a considerable linewidth loss.

It is assumed that the pattern transfer process is characterised by some constant over sizing or under sizing of the features delineated. This is expressed as a linewidth loss ( i.e. positive if undersized and negative if oversized ). In addition, it is assumed that the sheet resistivity of the N+ epi layer is essentially constant within the area occupied by the module.

The objective is to determine both the N+ epi sheet resistivity and the linewidth loss for the epi pattern transfer process ( which is performed before the epi receives the source/drain implant ). The method employed is similar to that used for the family of 4-terminal poly resistors.

The Van der Pauw resistor structure is included to provide a more direct measure of the sheet resistivity of the N+ epi. Whilst this structure is maximally tolerant to imperfections in the pattern transfer process used to delineate it, it is also rather insensitive. Consequently, it is more vulnerable to heating effects than the 4-terminal resistors. The Van der Pauw resistor structure employed is a Greek Cross design, with 10um wide arms. Since the Van der Pauw resistor allows the sheet resistivity to be measured within a highly localised area, it provides a valuable means of checking the sheet resistivity value derived from the conductance values for the four 4-terminal resistor structures.

Module 04, P+ Epi Bridge Resistor and Van der Pauw Structures

This module contains four 4-terminal resistors which differ only in that their nominal width is varied and a Van der Pauw resistor structure. The contacts required are formed directly below the probe access pads, using the largest dimensions possible in order to minimise their resistances.

The four 4-terminal resistors are similar to those employed in module 02 except that they are defined in P+ epi ( i.e. epi which has received the P channel source/drain implant ) instead of being defined in doped poly.

The distance between the voltage sensing taps is 100um. The width of the tracks used for the four P+ epi resistors are 5um, 10um, 15um and 20um respectively. The width of the voltage sensing taps employed is 2um.

It is assumed that the pattern transfer process is characterised by some constant over sizing or under sizing of the features delineated. This is expressed as a linewidth loss ( i.e. positive if undersized and negative if oversized ). In addition, it is assumed that the sheet resistivity of the P+ epi layer is essentially constant within the area occupied by the module.

The objective is to determine both the P+ epi sheet resistivity and the linewidth loss for the epi pattern transfer process ( which is performed before the epi receives the source/drain implant ). The method employed is similar to that used for the family of 4-terminal poly resistors.

The Van der Pauw resistor structure is included to provide a more direct measure of the sheet resistivity of the P+ epi. Whilst this structure is maximally tolerant to imperfections in the pattern transfer process used to delineate it, it is also rather insensitive. Consequently, it is more vulnerable to heating effects than the 4-terminal resistors. The Van der Pauw resistor structure employed is a Greek Cross design, with 10um wide arms. Since the Van der Pauw resistor allows the sheet resistivity to be measured within a highly localised area, it provides a valuable means of checking the sheet resistivity value derived from the conductance values for the four 4-terminal resistor structures.

Module 05, Poly Step Coverage Check and Van der Pauw Structures

This module contains two "step coverage check" structures plus three Van der Pauw resistor structures. The contacts necessary are formed directly below the probe access pads, using the largest dimensions permissible to minimise their resistances.

Each step coverage check structure consists of a pair of parallel tracks which are required to surmount a series of "steps", without resulting in breaks caused by step coverage problems or shorts due to fillets of poly left behind as a result of imperfect pattern transfer. One is defined on a planar surface to provide a reference whilst the other routes the poly tracks over a series of epi strips to produce a series of 100 steps. The poly tracks are 2um wide on a 5um pitch. The epi strips are 4um wide on an 8um pitch.

The objective is to check for step coverage or pattern transfer problems during processing. Breaks in the poly result in an open-circuit between the two ends of the track involved. Unintended poly fillets result in a higher conductance between the two tracks than expected ( the structure defined on a planar surface provides a reference conductance value ).

The three Van der Pauw resistor structures are defined in poly which has been very heavily doped with phosphorus ( i.e. N type ). Their design is identical to those used for the epi layer. One subsequently receives the N channel source/drain implant, one subsequently receives the P channel source/drain implant, whilst the third receives neither.

The objective is to evaluate the effect of the self-aligned source/drain implants on the sheet resistance of the poly layer. Whilst the majority of the poly receives neither implant, the gate electrodes of the devices will receive either additional N type dopant or a compensating dose of P type dopant when the self-aligned source/drain implants are performed.

Module 06, Metal Step Coverage Check Structures

This module contains five "step coverage check" structures. Rugged probe access pads are provided by defining isolated islands of poly ( directly below the pads ) and forming a contact between them by using the largest contact hole dimensions possible.

Each step coverage check structure consists of a pair of parallel tracks which are required to surmount a series of "steps", without resulting in breaks, caused by step coverage problems, or shorts due to metal fillets left behind as a result of imperfect pattern transfer. Two of these step coverage check structures are defined on a planar surface ( no "steps" ) to provide a reference, whilst the other three use strips of epi, strips of poly and trenches defined in the flow glass respectively to produce a series of 100 "steps" to be crossed. The metal tracks are 4um wide on an 8um pitch for all five structures. The strips of epi for the metal over over epi structure are 4um wide on an 8um pitch. The strips of poly for the metal over poly structure are 4um wide on an 8um pitch. The trenches defined in the flow glass for the metal over contact trench are 6um wide on a 10um pitch.

The objective is to check for step coverage or pattern transfer problems

during processing. Breaks in the metal result in an open-circuit between the two ends of the track involved. Unintended metal fillets result in a higher conductance between the two tracks than expected ( the structures defined on a planar surface provide a reference conductance value ).

Module 07, Transmission Line Tapped Resistors and Contact Chains

This module contains a Transmission Line Tapped Resistor structure and a Contact Chain structure for each of the three kinds of contact formed by the process. Namely, contacts to N+ epi, contacts to P+ epi and contacts to poly. The poly areas contacted are heavily doped N type, but have not received either of the self-aligned source/drain implant doses. The test structures for the poly contacts have been duplicated. The probe access pads have been ruggedised in the customary manner.

The design of the Transmission Line Tapped Resistor structures is rather unconventional. Connections are made to the contacts via a single probe access pad rather than the customary Kelvin connection. This economy of probe access pad utilisation is bought at the expense of accuracy, since the front resistance value derived will include a contribution caused by the non-zero resistance of the probe. Two pairs of contacts are normally used. The separation between the front edges of the contacts is small in one case and large in the other. The front resistance and the resistance per unit length of the semiconductor track contacted can then be derived by solving a pair of simultaneous equations. This assumes that all three contacts employed are identical. By using three pairs of contacts, where the separation between front edges is varied, it is possible to check if this assumption is valid or not.

The front resistance for the contact is derived from the TLTR structure. Three current paths exist, in which current flows through a known length of the semiconductor track via an adjacent pair of contacts. If all four contacts are assumed to be identical, then it is possible to derive both the front resistance and the resistance per unit length by measuring the 2-terminal resistances for these three paths and fitting a least squares straight line to the resistance values against the distance between the front edges for the corresponding contact pairs. The linear correlation coefficient for this least squares fit can be used to check the validity of the assumption made.

The nominal dimensions of the contacts employed are 6um long by 6um wide ( i.e. the smallest allowed by the design rules ) and the semiconductor tracks contacted are 10um wide. The contacts of the TLTR structures are defined so that the distances between the front edges of the three pairs of adjacent contacts are 30um, 60um and 90um respectively.

The Contact Chain structures contain a chain of 100 contacts. They have been included merely to establish how likely it is that other structures will fall victim to open-circuit contacts.

Module 08, Inter-layer Misalignment Measurement Structures, set A

This module contains two structures to detect alignment error due to the DSW lithography machine. One structure is designed to sense misalignment of the contact holes to the underlying epi layer. The other is designed to sense misalignment of the metal to the underlying epi layer. The epi areas defined for this module receive the N channel source/drain implant to ensure that they are sufficiently conductive.

These structures employ a "differential potentiometer", which produces a voltage that is proportional to the displacement of one "wiper" relative to the other. The "wipers" sense the potential along two parallel strips of epi whose widths are constant. The "wiper" for one potentiometer is a voltage sensing tap midway along its epi strip whilst the "wiper" of the other potentiometer is a metal to epi contact instead. If the centre of the contact lies on the centre-line of the voltage sensing tap, then the potential difference between the "wipers" will be zero. However, if the centre of the contact is displaced at right angles to the centre-line of the voltage sensing tap, then the potential difference between them will be proportional to the displacement. If two "differential potentiometer" structures are used for each axis, where the centres of the contacts are each offset by 1um in opposite directions, then the alignment errors can be determined.

The voltage sensing contact of the "differential potentiometers" used to measure the contact hole to epi alignment error is 6um square. The metal layer overlap margin for this contact is sufficiently large to guarantee that the contact area is defined by the contact hole.

The voltage sensing contact of the "differential potentiometers" used to measure the metal to epi alignment error is 6um by 20um in the direction of current flow. The contact is formed between a 4um wide metal "finger" and the epi exposed by the contact hole. The position of this contact is thus determined by the alignment of the metal relative to the underlying epi, rather than by the position of the contact hole.

Module J9, Inter-layer Misalignment Measurement Structures, set B

This module contains two structures to detect alignment error due to the DSW lithography machine. One structure is designed to sense misalignment of the contact holes to the underlying poly layer. The other is designed to sense misalignment of the poly to the underlying epi layer.

The structure used to measure the misalignment of the contact hole layer to the poly layer is similar to that used to measure the misalignment of the contact hole layer to the epi layer. It merely uses poly rather than epi.

The structure designed to sense poly to epi misalignment takes advantage of the self-aligned source/drain implant. The pattern defined in the epi layer is such that if a rectangular segment is subsequently removed, two 4-terminal resistor structures would be left. Since the process does not facilitate the removal of this segment, it is masked by a poly electrode such that only those areas necessary to realise the 4-terminal resistors receive the self-aligned N channel source/drain implant. By biasing this gate electrode to deplete the underlying channel region, the rectangular segment is effectively removed. The design of the structure is such that the difference between the effective widths for the 4-terminal resistors will be proportional to the misalignment of the poly with respect to the epi in one axis only. Evidently, separate structures are needed for each axis. Unfortunately, the calibration of this structure will be affected by linewidth losses introduced by both the epi and poly pattern transfer processes and by lateral diffusion of the source/drain implant. Too many probe access pads would be necessary in order to implement a methodology similar to that used for the "differential potentiometer" structures. It is noted, however, that the misalignment of the poly relative to the epi can be deduced from the difference between the contact to poly alignment error and the contact to epi alignment error.

Module 10, Gate Oxide Capacitor Structures

This module contains four "rectangular" capacitor structures whose areas are well defined, but which are expected to be of limited use since they will have a large parasitic series resistance to the lower electrode. It also contains four "interdigitated" capacitor structures which have been designed so that the parasitic series resistance is less. This reduction is achieved at the expense of a less well defined area plus an increased capacitance due to peripheral effects.

The "rectangular" capacitor structure is a parallel plate capacitor. The area of the capacitor and its periphery are determined by the dimensions of the upper electrode, which is defined in poly. This capacitor has an effective area of 39,450 square microns and a periphery of 1010 microns. The underlying epi extends beyond the edges of the poly electrode and is implanted using one of the source/drain implants. This peripheral region supplies the carriers necessary to form an inversion layer when the poly electrode is biased appropriately. Two of the four rectangular capacitor structures receive the N channel source/drain implant. They also receive the N channel threshold adjustment and back-channel suppression implants so that the epi which forms the lower electrode is the same as that used for the channel region of an N channel device. The other two rectangular capacitor structures receive the P channel source/drain implant instead. They do not receive any other implants so that the epi which forms their lower electrodes is the same as that used for a P channel device.

The objective is to evaluate the capacitance per unit area figure needed to calculate the effective carrier mobility exhibited by N and P channel devices and to determine the breakdown voltage for the gate oxide.

The "interdigitated" capacitor structures are designed to minimise their series resistance. The poly electrode is comb-shaped and is placed above a rectangle of epi so that the source/drain implant produces a series of low resistivity regions. Contacts are formed between these regions and a comb-shaped metal pattern. This reduces the parasitic series resistance.

The N channel source/drain implant is used for two of the interdigitated capacitor structures. One of them receives both the N channel threshold adjustment and back-channel suppression implants and the other does not. The P channel source/drain implant is used for the other two structures. Neither of them receive any other implant.

The objective is to provide structures suitable for C/V measurements. It is questionable whether it is possible to obtain useful information from these structures or not. This is because it is probable that the overlap capacitance will be larger than the depletion layer capacitance when the poly gate is biased to deplete the surface. In addition, it is probable that epi will become fully depleted, so that it is impossible to obtain useful C/V data.

Module 11, N and P Channel Annular Devices

This module contains a pair of N channel annular device structures and a pair of P channel annular device structures. One of each pair of devices has an annular ring that is complete, in order to eliminate the sidewall normally present, whilst the other has a slot cut into the annular ring. Thus, one structure is free of the effects of parasitic sidewall devices whilst the other is not.

Regular 20 sided polygons are used instead of true circles in the design of the annular device structures. The inner radius of the gate electrode is 14um and the outer radius is 26um. It is necessary to violate several design rules in order to realise these structures because the contact to the gate electrode must be defined directly above the channel region and because the metal track which connects the innermost source/drain region to its probe access pad must cross the poly gate electrode.

The objective is to make it possible to discriminate between leakage due to the existence of a parasitic back-channel and leakage attributable to the parasitic sidewall devices ( although the sidewall devices should be affected by the gate potential whilst the back-channel should not ).

Module 12, Long N and P Channel Devices

This module contains three rectangular N channel and three rectangular P channel devices of varied width. The length of these devices is expected to be sufficient to ensure that long channel approximations describe the characteristics accurately. Dedicated probe access pads are provided to ensure that there can be no interaction between the devices.

Both sets of devices are 40um long. The widths are 10um, 130um and 250um respectively. The contacts to source, gate and drain are 6um long and as wide as possible.

The objective is to synthesise the characteristics of a 40um long, 240um wide, "edgeless" device by taking the difference between the current for the 250um wide device and the 10um wide device, where both currents have been measured with identical bias conditions. This pseudo-device serves the same function as the edgeless annular device structure in module 11. The characteristics of a 40um long, 120um wide device can be synthesised in a similar manner either by using the 130um wide and 10um wide devices or by using the 250um wide and the 130um wide devices instead. Thus, it is possible to test the validity of the assumptions made.

Modules 13 and 14, Devices With Varied Orientation

These modules contain four rectangular devices which differ only in that direction of current flow is at either 0 degrees, 45 degrees, 90 degrees or 135 degrees to the X axis. Each device is 50um long by 50um wide and has a voltage sensing tap halfway down each side. Dedicated probe access pads are provided to ensure that the can be no interaction between them.

Module 13 contains a set of N channel devices, whilst module 14 contains a set of P channel devices.

The objective is to investigate variations in carrier mobility exhibited by devices for which the direction of current flow is varied.

Modules 15 to 22, Families of Devices With Varied Length

Each of these modules contains a family of six devices which differ only in that the widths of their polysilicon gate electrodes are varied. This is ensured by utilising the "rubber-banding" capability of the CAD suite to "stretch" the channel region of a notional device as required. These modules also include a two terminal device structure, where the width of the poly gate electrode has been shrunk to zero. Dedicated probe access pads are provided for each structure in order to ensure that there is no interaction between them.

Module 15 contains a family of 10um wide N channel devices whose lengths are 1um, 2um, 3um, 4um, 5um and 10um respectively. Module 16 is similar, except that the devices are P channel instead. The nominal channel width of 10um corresponds to the minimum width, for which a rectangular active area can be defined. This is dictated by the minimum dimensions for the contacts and the margin required to provide tolerance to misalignment of the contact layer to the underlying layers.

Module 17 contains a family of 2um wide N channel devices whose lengths are 1um, 2um, 3um, 4um, 5um and 10um respectively. Module 18 is similar, except that the devices are P channel instead. The active area for these modules is dumbell-shaped. The source and drain contacts are centred on 10um square areas which are joined by a 2um wide strip. In order to make sure that these structures are tolerant to misalignment of the poly gate layer to the active area regions, this 2um wide strip is extended by 1um at each end. Thus, the active area region for the "zero-length device" structure is also dumbell-shaped.

Module 19 contains a family of 40um wide N channel devices whose lengths are 1um, 2um, 3um, 4um, 5um and 10um respectively. Module 20 is similar, except that the devices are P channel instead. The width of the contacts to the source and drain regions are made as wide as possible in order to minimise the resistances associated with them.

Module 21 contains a family of 10um wide N channel devices whose lengths are 2.5um, 2.7um, 2.9um, 3.1um, 3.3um and 3.5um respectively. Module 22 is similiar except that the devices are P channel instead.

The objective is to investigate the variation observed in the parameters of the generic equations used to describe the device characteristics, as the nominal channel length is varied. The families of 40um wide devices are intended to minimise the effect of any parasitic sidewall devices by maximising the ratio of the width of the surface channel to the width of the parasitic sidewall devices. Conversely, the families of devices with nominal widths of 2um are intended to highlight the effects of parasitic sidewall devices.

Modules 23 to 26, Families of Devices With Varied Width

These modules each contain a family of devices whose width is varied. In order to be able to allow for the effect of the different contact widths for these devices, Kelvin connections are made to their source and drain regions. Dedicated probe access pads are provided for each structure to ensure that there is no interaction between them.

Module 23 contains a family of 3um long N channel devices with widths of 10um, 20um, 30um and 40um respectively. Module 24 is similar except that it contains a family of P channel devices instead.

Module 25 contains a family of 3um long N channel devices with widths of 2um, 4um, 6um and 8um respectively. The devices all have dumbell-shaped active area regions, similar to those employed in the families of narrow devices of varied length. Module 26 is similar to module 25, except that the devices are P channel instead.

The objective is to investigate the variation observed in the parameters

of the generic equations used to describe the device characteristics, as the width of the channel is varied. The device structures employed have the virtue that it is possible to evaluate their characteristics despite high resistance or even non-ohmic contacts.

Modules 27 and 28, Devices In Close Proximity

These modules contain a set of eighteen nominally identical devices with common gate and common source connections. The common gate connection is made to a poly track which crosses all eighteen teeth of the comb-shaped active area region and the common source connection is made via a single wide contact to the active area region.

Module 27 contains nominally identical, 3um long by 10um wide, N channel devices, whilst module 28 contains nominally identical, 3um long by 10um wide, P channel devices instead.

The objective is to evaluate the variation in the device parameters that occur within a localised area.

Module 29, Gate Controlled Van der Pauw Structures of Varied Orientation

This module contains four gate controlled Van der Pauw structures. These VDP structures are designed with corner contacts. The surface potential of the epi is controlled by the potential applied to the gate electrode. Two of these structures receive both of the N channel implant doses plus the self-aligned N channel source/drain implant whilst the two remaining structures receive the self-aligned P channel source/drain implant only. One of each pair of gate controlled Van der Pauw resistors is rotated by 45 degrees relative to the other, so that the sensitivity to orientation can be investigated.

The objective is to investigate the variation in the conductivity of the inversion layer formed when the gate is biased appropriately and also to reveal variation in the carrier mobility exhibited when the direction of current flow is altered.

Module 30, Substrate Contacted Devices

This module contains two N channel and two P channel devices whose width is defined by a channel-stop implant. The N channel source/drain implant is used as the channel-stop implant for the P channel devices whilst the P channel source/drain implant is used as the channel-stop for N channel devices. The shape of the gate electrode is designed to ensure that both implants can be self-aligned to the gate, whilst allowing for worst-case misalignment of the implant masks to the underlying features. Separate contacts are formed to the channel-stopped regions on either side of the channel. If a conductive path exists between these two regions, then it is likely that the substrate potential can be pinned as required.

The two N channel devices and the two P channel devices included in this module are all 20um long and are either 2um or 10um wide.

The objective is to facilitate an investigation of the kink effect. This is usually attributed to the fact that the substrate is allowed to float in SOS device structures. These structure have been included so that the device characteristics when the substrate is pinned to a known potential can be compared with those obtained when it is allowed to float.

Module 31, Hall Bar Structures

This module contains two Hall Bar structures, one for N channel material and another for P channel material. Each Hall Bar structure consists of a long, wide FET with three voltage sensing taps defined on either side.

The channel region for these structures is 250um long by 50um wide. Taps are provided half way down each side and additional taps are provided at 50um on either side of the central taps. All six taps are 5um wide.

The objective is to integrate the structures required to investigate the mobility dependences ( by using Hall measurement equipment ) on the same chip as that used for routine measurements.

Module 32, Miscellaneous Circuit Elements

This module contains an inverter, a transmission gate, and an output pad driver which are all utilised in the design of the 16 bit shift register included in module 33. It also contains a 3-input NOR gate ( to make use of the remaining probe access pads ). These circuits utilise 6um square contacts. Where N and P channel source or drain regions are connected to one another, the active areas are butted and a contact is placed so that the junction is short-circuited.

The inverter utilises 3um long, 10um wide, N and P channel devices. This is evidently not an optimum design. The transmission gate also utilises 3um long, 10um wide, N and P channel devices and includes an inverter to provide the complementary clock drive required. The output pad driver is made up of two inverter stages. The first stage employs 3um long devices where the N channel device is 56um wide and the P channel device is 76um wide. The second stage employs three devices, similar to the devices for the first stage, connected in parallel to increase the drive capability. The 3-input NOR gate employs N and P channel devices, which are 3um long and 10um wide.

The objective is to evaluate the transfer characteristics of the circuit elements used in the design of the 16 bit serial input, parallel output, synchronous shift register included in module 33.

Module 33, 16 Bit Synchronous Shift Register Circuit

This module contains a 16 stage synchronous shift register with a serial input and parallel outputs. Each stage comprise a master/slave flip-flop realised using a pair of inverters with transmission gates to enable the feed-back and feed-forward signal paths. The basic building blocks used in this design are included in module 32.

The objective is to determine the maximum clock rate that can be applied before the circuit ceases to function properly, by using a fast external divide by sixteen circuit to provide the input signal and then examining both the input and the output waveforms. The shift register approach has the advantage that the critical waveforms are relatively slow ( compared to, say, a ring oscillator ).

Unfortunately, a number of errors were made when defining the layout for this circuit. They are so severe that there is absolutely no chance that it might work. These errors have since been corrected, but both the 8501 and the 8502 mask sets remain defective in this respect.

Module 34, Various 3-input Gates

This module contains six different 3-input gates, originally laid-out as an exercise to evaluate the packing density achievable for random logic. It has only been included to fill an otherwise vacant space.

Modules 35 to 37, Sub-micron Channel Length Devices

These three modules are only realised when the E-beam lithography option for the 8502 mask set is employed. In this case, the superior resolution afforded by direct write on wafer, electron beam lithography is utilised to produce devices with sub-micron channel lengths by drawing sub-micron wide gate electrodes. For convenience, all of the features to be defined in the poly layer are drawn by E-beam using a tri-layer pattern transfer method.

Module 35 contains three N channel devices plus three P channel devices. The devices are all 10um wide and have nominal lengths of 1.00um, 0.75um and 0.50um respectively.

Module 36 is similar to module 35, except that the devices are 2um wide.

Module 37 is similar to module 36, except that devices have even shorter nominal channel lengths of 0.50um, 0.375um and 0.25um respectively.

The objective is to investigate the characteristics exhibited by devices with sub-micron channel lengths and thereby discover the minimum channel length possible.

# REPORT DOCUMENTATION PAGE

DRIC Reference Number (if known) .....

Overall security classification of sheet .....Unclassified.....

(As far as possible this sheet should contain only unclassified information. If it is necessary to enter classified information, the field concerned must be marked to indicate the classification eg (R), (C) or (S).

| Originators Reference/Report No. | Month | Year |
|---|---|---|
| MEMO 4369 | FEBRUARY | 1990 |

Originators Name and Location
RSRE, St Andrews Road
Malvern, Worcs WR14 3PS

Monitoring Agency Name and Location

Title
PARAMETRIC TESTING FOR THE RSRE CMOS, SILICON ON SAPPHIRE PROCESS

| Report Security Classification | Title Classification (U, R, C or S) |
|---|---|
| Unclassified | U |

Foreign Language Title (in the case of translations)

Conference Details

| Agency Reference | Contract Number and Period |
|---|---|
| | |

| Project Number | Other References |
|---|---|
| | |

| Authors | Pagination and Ref |
|---|---|
| BOLLER, D J | 58 |

Abstract

This memorandum describes the use of a purpose designed test chip and an unconventional parametric testing methodology to evaluate the outcome of an in-house CMOS, silicon on sapphire process.

Abstract Classification (U,R,C or S)
U

Descriptors

Distribution Statement (Enter any limitations on the distribution of the document)
Unlimited